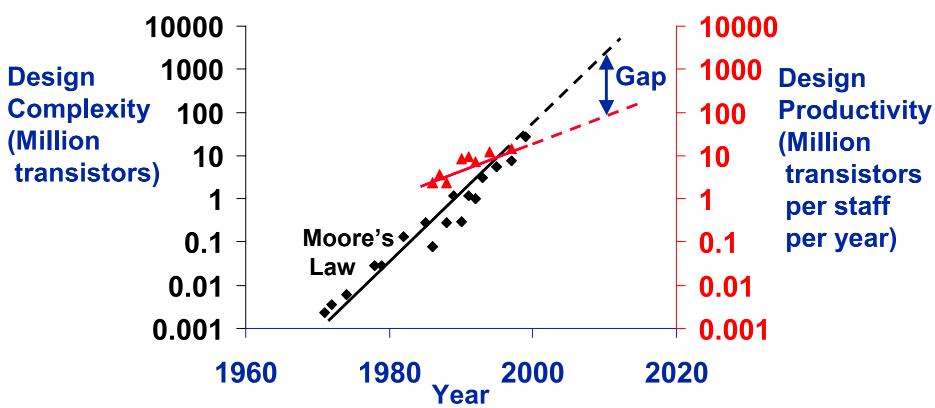
System-Level Modeling and Design of Integrated MEMS

Tamal Mukherjee
Department of Electrical and Computer Engineering
Carnegie Mellon University

tamal@ece.cmu.edu
http://www.ece.cmu.edu/~mems

NSF Summer School on
Computational Approaches for Simulation of MEMS,
Friday, May 24

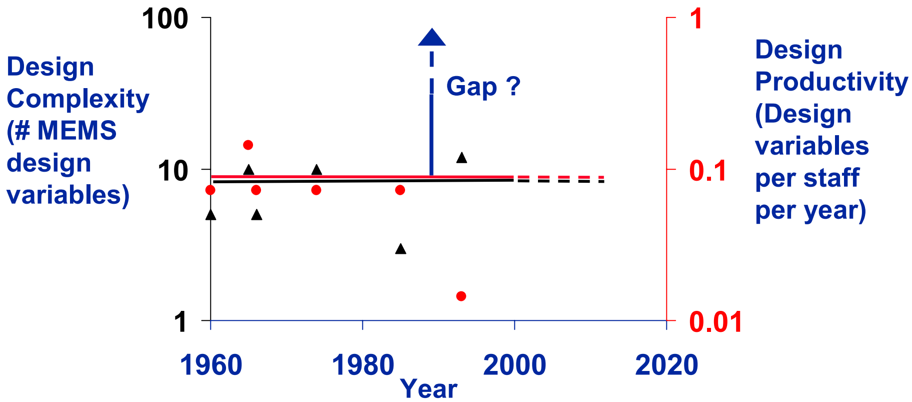
System Design Bottleneck



- **Increasing gap between technology advancement and ability to design new systems [SIA]**
- **Design team sizes need to increase to eliminate gap**

c. Carnegie Mellon

MEMS Design Bottleneck ?



- Same bottleneck, different scale
- How do we get design productivity to increase, so complexity can increase?

c. Carnegie Mellon

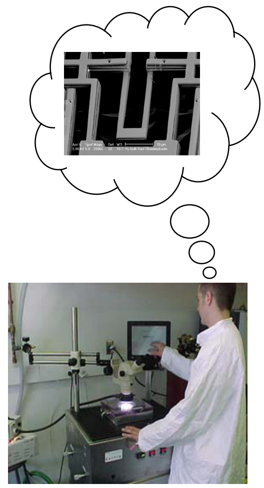
Outline

- MEMS Design Issues
- Process & Design Abstractions
- MEMS Circuit Level Modeling & Simulation
- Layout Generation
- Layout Verification
- Mesh Generation
- Synthesis
- Summary

c. Carnegie Mellon

Today's MEMS Designers

- Process flow
- Materials characterization

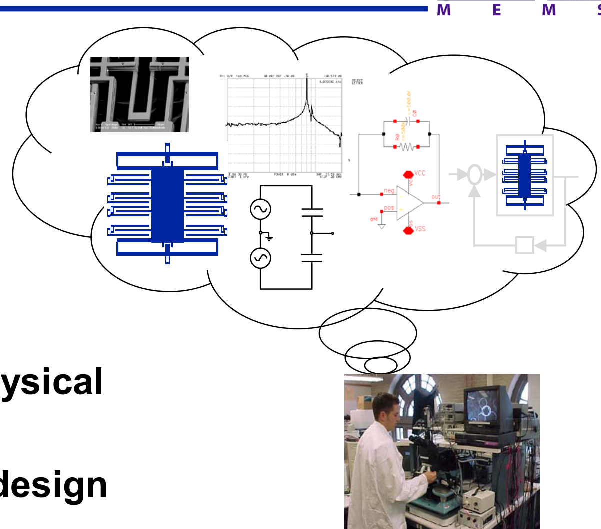


1) Process design

c. Carnegie Mellon

Today's MEMS Designers

- Process flow
- Materials characterization

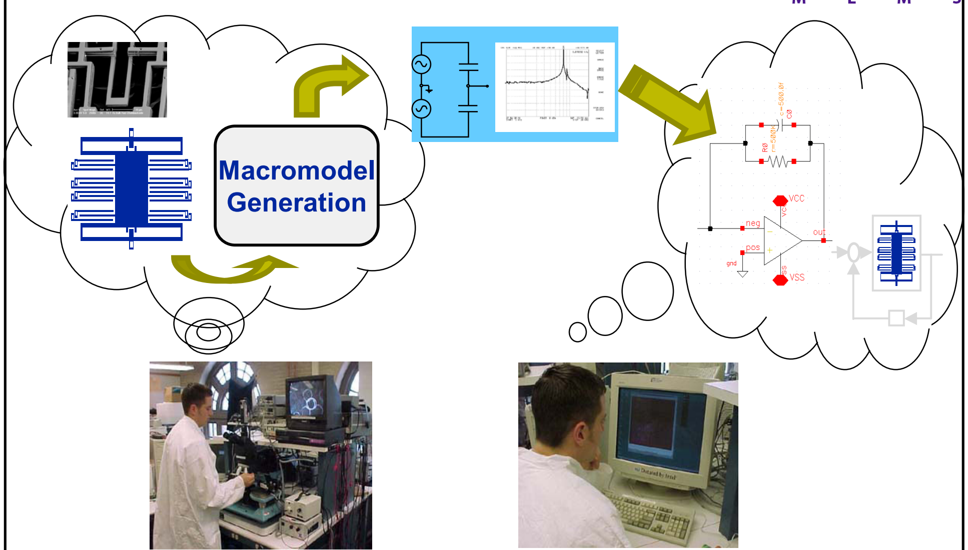


- **Modeling of physical interactions**
- **Layout-based design**
- **Interface circuits**

2) Component design

c. Carnegie Mellon

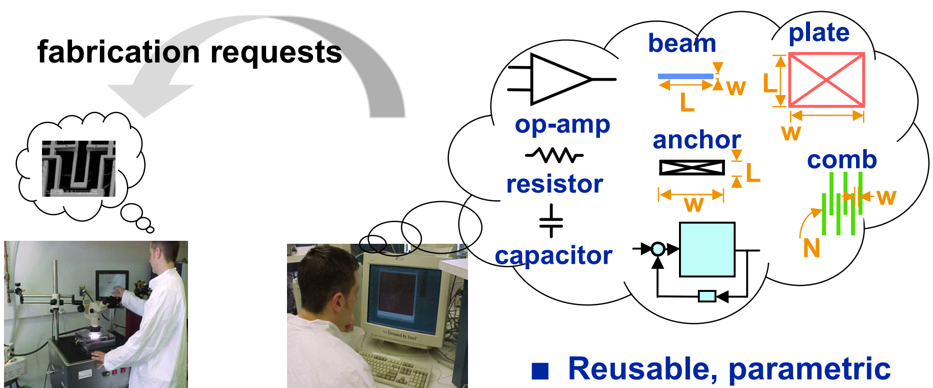
Bottom-Up Design



Device design

System design

Top-Down Design



Foundry

Application-Specific Design

design rules,
material parameters,
device models

- Reusable, parametric models
- Macromodel bottleneck moved to library creation, and removed from design iteration

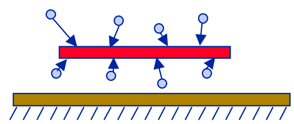
MEMS Design Issues

- Layout
  - Will it release ?
  - Will it function ?
  - Will it meet specifications ?
    - Dynamic range
    - Sensitivity (parasitics)
    - Sensor resolution (noise)
- Design
  - Interface circuits
  - Electromechanical feedback systems
  - Device matching
  - Design for manufacturability, testability
    - minimize sensitivity to variations
    - account for device calibration

e.g.

Brownian noise

$$\sqrt{F_n^2} = \sqrt{4k_BT\,B\,\Delta f}$$



➔ Requires hierarchical design methodology

c. Carnegie Mellon

Integrated MEMS Design

- Application Driven $\Rightarrow$ Low-volume custom MEMS
- Design Methodology Characteristics
  - Support wide variety of MEMS fab processes
  - Supporting a wide class of MEMS designs
  - Extensible to new MEMS design concepts
  - Fits into the existing VLSI design flows
  - Capable of evaluating integrated system designs

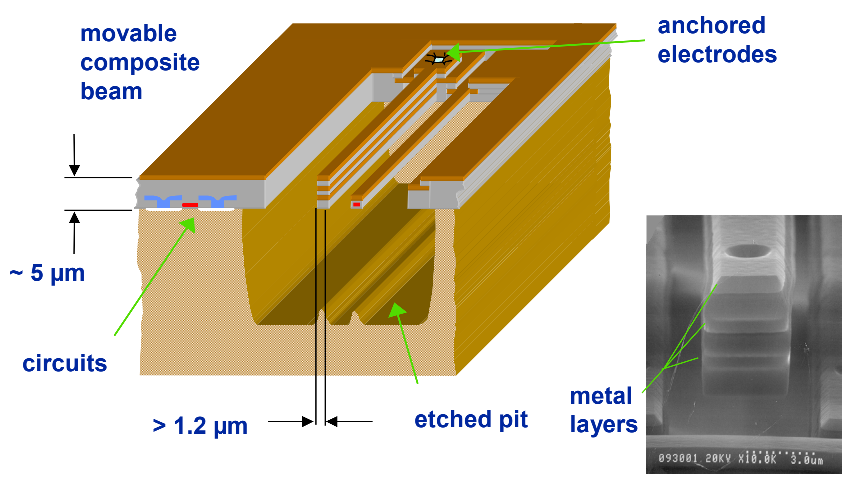
c. Carnegie Mellon

Outline

- MEMS Design Issues
- **Process & Design Abstractions**
- MEMS Circuit Level Modeling & Simulation
- Layout Generation
- Layout Verification
- Mesh Generation
- Synthesis
- Summary

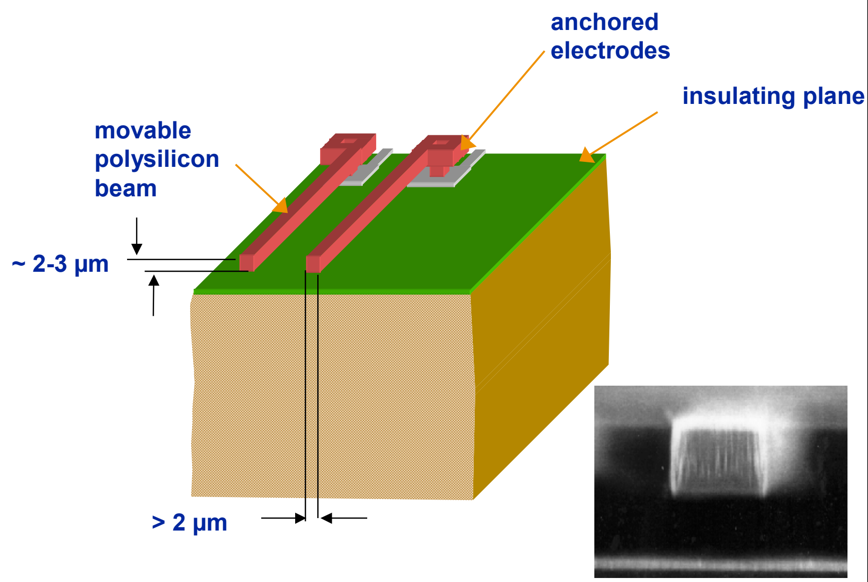
c. Carnegie Mellon

Process Abstractions: CMOS Micromachining



c. Carnegie Mellon

Process Abstractions: Polysilicon Micromachining



c. Carnegie Mellon

Process Abstractions: Technology Capture

- Decoupling of process complexity and design complexity through process abstraction
- MEMS processing derived from VLSI
- Use VLSI process abstractions
  - Layout technology file
  - Model technology file
  - Design rule file
  - Layout (parasitic) extraction file

c. Carnegie Mellon

Process Abstractions: Layout Technology File

- Same as VLSI
- Interface to foundry
- Layer definition
  - GDS number
- Layer order
- Not required for simulation

```
(("Nwell" "drawing")   42   0   t)
(("Active" "drawing")  43   0   t)
...
(("Poly1" "drawing")   46   0   t)
(("P1Con" "drawing")   47   0   t)
(("Metal1" "drawing")  49   0   t)
(("Metal2" "drawing")  51   0   t)
```

```
(("POLY0" "drawing")   13   0   t)
(("HOLE0" "drawing")   41   0   t)
(("POLY1" "drawing")   45   0   t)
(("ANCHOR1" "drawing") 43   0   t)
(("HOLE1" "drawing")   44   0   t)
(("POLY2" "drawing")   49   0   t)
(("HOLE2" "drawing")   46   0   t)
...
```

c. Carnegie Mellon

Process Abstractions: Model Technology File

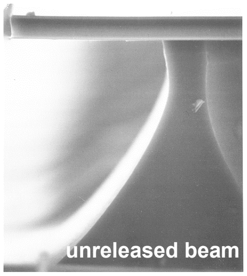
- Process-dependent information
  - Layer thicknesses
  - Material properties
- Parameters common to all models in element library

```
`define m1_resistivity        0.07
`define m1_thickness          0.7u
`define m1_density            2700
`define spacer_gap            20u
`define E                     62G
`define stress                300M
`define stress_gradient       10M
```

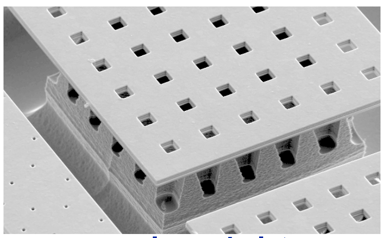
```
`define poly1_resistivity     10
`define poly1_thickness       2u
`define poly1_density         2330
`define spacer_gap            2u
`define E                     165G
`define stress                3M
`define stress_gradient       0.1M
```

c. Carnegie Mellon

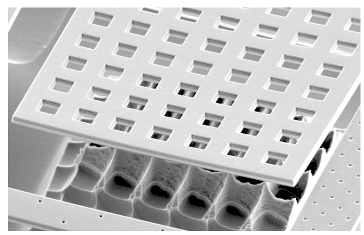
Process Abstractions: Design Rule Check



- MEMS introduces
  - Sacrificial etch to release structure
- Microstructure release of depends on
  - Gap size
  - Gap shape
  - Gap spatial distribution



unreleased plate

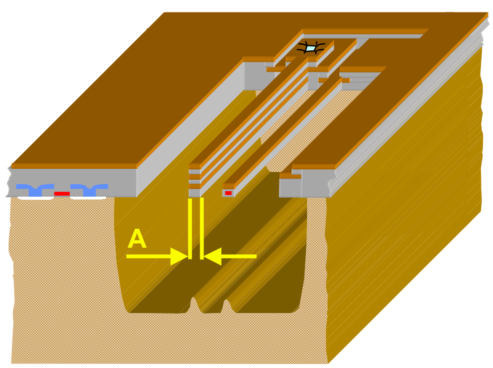


released plate

c. Carnegie Mellon

Process Abstractions: MEMS-Specific Design Rules

- MEMS release step adds new constraints on design rules



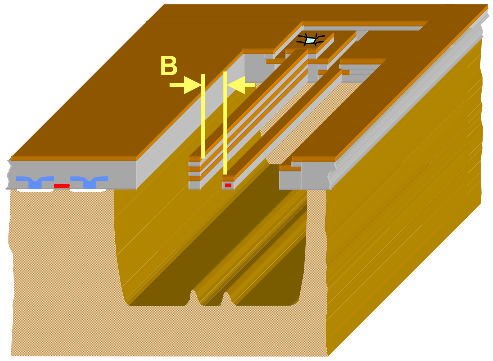
- CMOS-MEMS Example:

  A – Minimum and maximum structural width

c. Carnegie Mellon

Process Abstractions: MEMS-Specific Design Rules

- MEMS release step adds new constraints on design rules

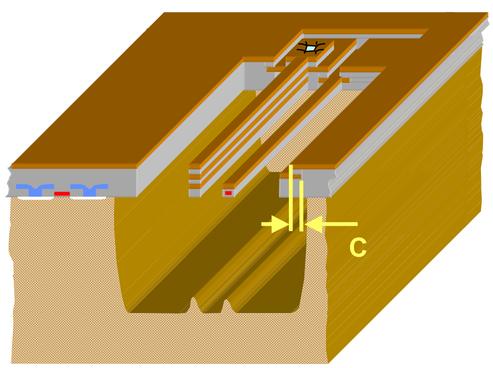


- CMOS-MEMS Example:
  - A – Minimum and maximum structural width
  - B – Minimum gap between structures

c. Carnegie Mellon

Process Abstractions: MEMS-Specific Design Rules

- MEMS release step adds new constraints on design rules

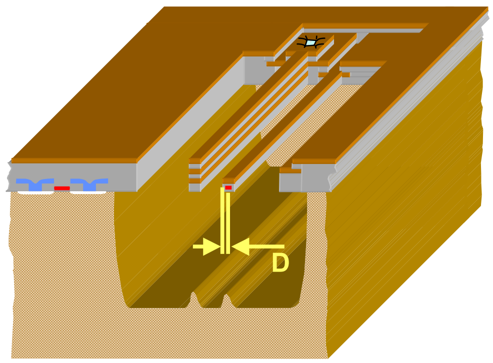


- CMOS-MEMS Example:
  - A – Minimum and maximum structural width
  - B – Minimum gap between structures
  - C – Minimum structural metal extension

c. Carnegie Mellon

Process Abstractions: MEMS-Specific Design Rules

- MEMS release step adds new constraints on design rules

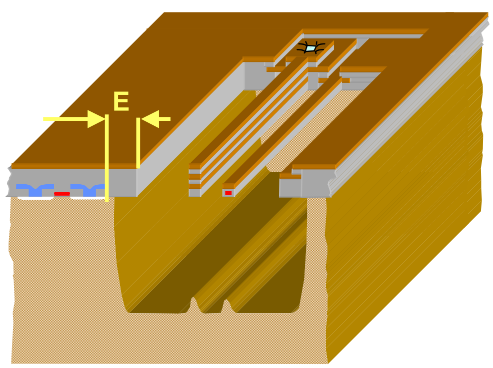


- CMOS-MEMS Example:
  - A – Minimum and maximum structural width
  - B – Minimum gap between structures
  - C – Minimum structural metal extension
  - D – Minimum polysilicon spacing from edge

c. Carnegie Mellon

Process Abstractions: MEMS-Specific Design Rules

- MEMS release step adds new constraints on design rules



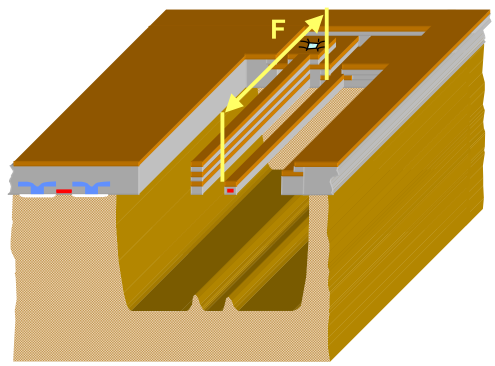
- CMOS-MEMS Example:

A – Minimum and maximum structural width
B – Minimum gap between structures
C – Minimum structural metal extension
D – Minimum polysilicon spacing from edge
E – Minimum electronics spacing from edge

c. Carnegie Mellon

Process Abstractions: MEMS-Specific Design Rules

- MEMS release step adds new constraints on design rules

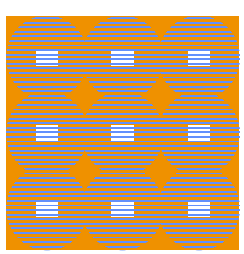


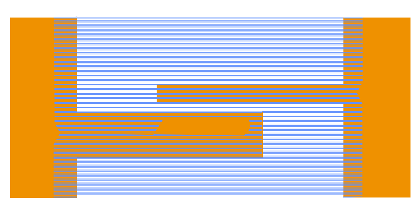
- CMOS-MEMS Example:
  - A – Minimum and maximum structural width
  - B – Minimum gap between structures
  - C – Minimum structural metal extension
  - D – Minimum polysilicon spacing from edge
  - E – Minimum electronics spacing from edge
  - F – Maximum beam length

c. Carnegie Mellon

Process Abstractions: MEMS DRC – "One Size Doesn't Fit All"

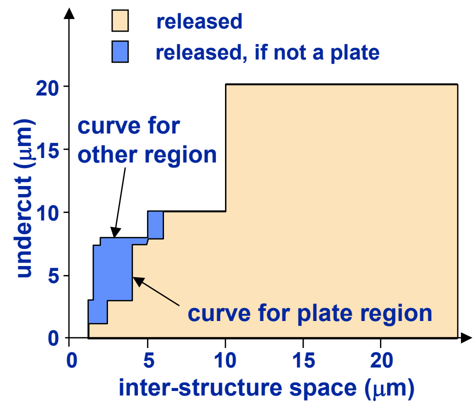
- Minimum possible gap
  - Function of adjacent structural width
  - Etch rate depends on local neighborhood
- Structural design issues
  - Narrow gaps desired for actuation
  - Wide structures desired for rigidity and wiring
- Desire context-dependent DRC





c. Carnegie Mellon

Process Abstractions: Context Dependent DRC

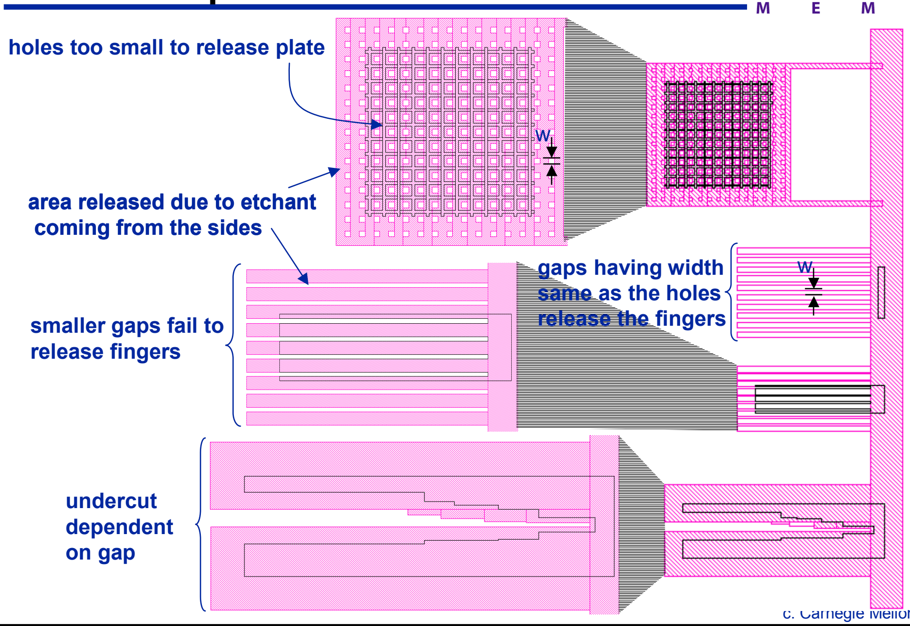


- Etch rate different for plate and non-plate regions
- MEMS areas recognized by maximum etch criterion
- Released areas found by emulating etch phenomenon

B. Baidya *et al.*, MSM 2001

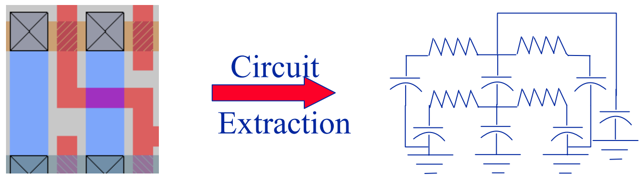
c. Carnegie Mellon

Process Abstractions: Context Dependent DRC

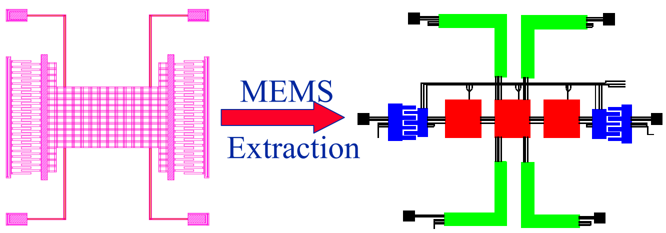


c. Carnegie Mellon

Process Abstractions: Layout Parasitic Extraction



- •Recognizes layer overlaps and gaps
- •Capacitors, resistors and transistors

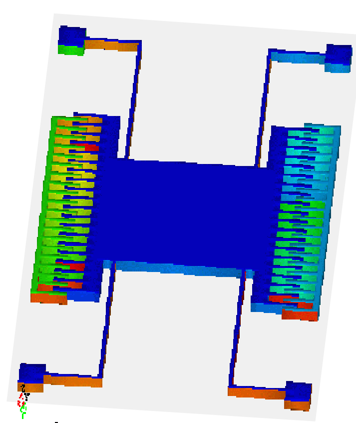


- •Recognizes layer overlaps, gaps and geometrical features
- •Springs, plates, comb drives

c. Carnegie Mellon

Design Representations

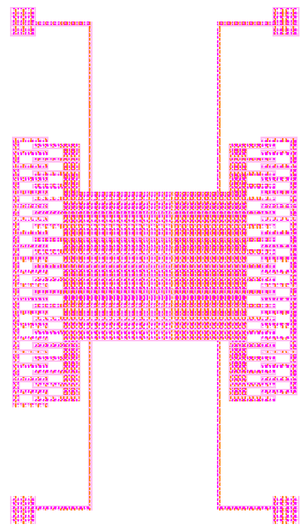
- 3D Representations
  - Solid Model
  - Mesh
  - Original Design Entry Mode



c. Carnegie Mellon

Design Representations

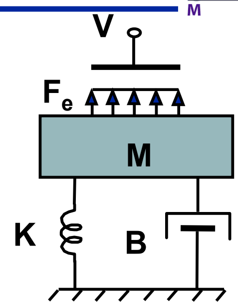
- 3D Representations
  - Solid Model
  - Mesh
  - Original Design Entry Mode
- Layout
  - VLSI fabrication
  - Preferred Design Entry Mode



c. Carnegie Mellon

Design Representations

- 3D Representations
  - Solid Model
  - Mesh
  - Original Design Entry Mode
- Layout
  - VLSI fabrication
  - Preferred Design Entry Mode
- Behavioral Schematic

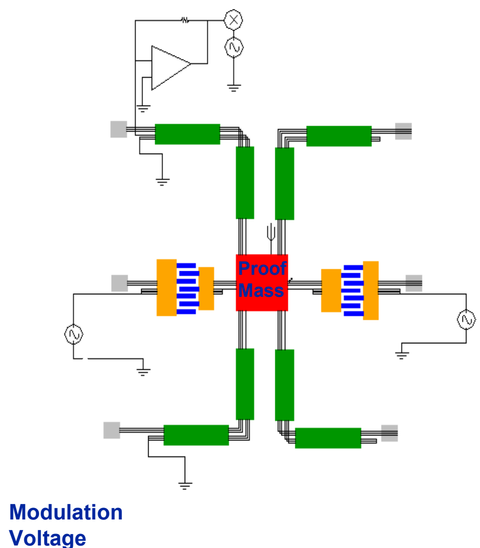



```
module resonator(vin);
…
parameter real  K = 1 ;
parameter real  B = 1e-7 ;
…
analog begin

Pos(Vtop) <+  ddt(Pos(top));
Pos(Atop) <+  ddt(Pos(Vtop));
Fe = (V(vin)*V(vin))*area*`eps0/2.0/
      ((z0-Pos(top))*(z0-Pos(top)));
F(top) <+ Fe -
   (K*Pos(top) + ms*Pos(Atop) +
B*Pos(Vtop));

end
endmodule
```

c. Carnegie Mellon

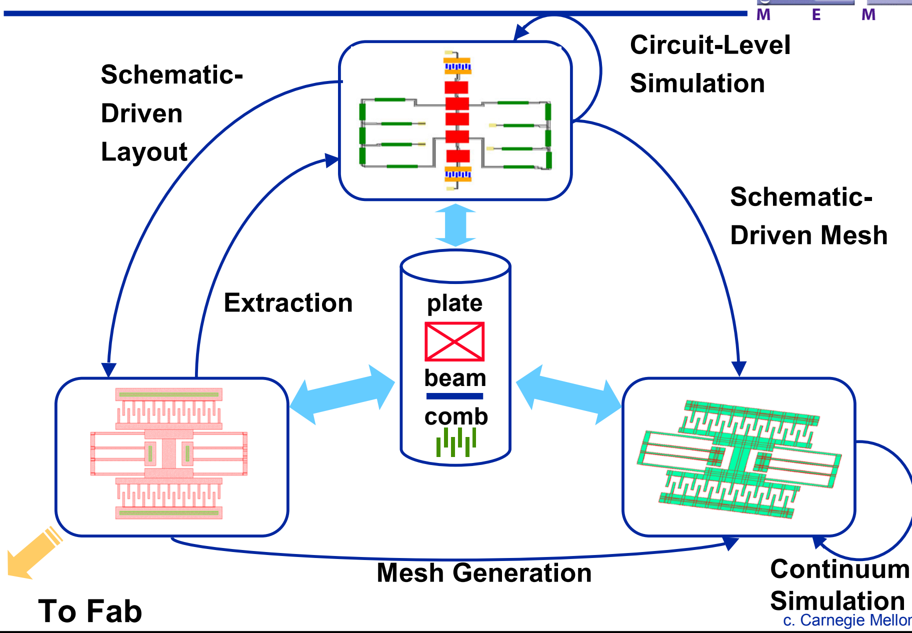
Design Representations

- 3D Representations
  - Solid Model
  - Mesh
  - Original Design Entry Mode
- Layout
  - VLSI fabrication
  - Preferred Design Entry Mode
- Behavioral Schematic
- Circuit-level Schematic
  - One-on-One Correspondence to Layout



c. Carnegie Mellon

Design Representation Links



c. Carnegie Mellon

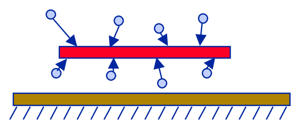
MEMS Design Issues

- Will it meet specifications ?
  - Dynamic range
  - Sensitivity (parasitics)
  - Sensor resolution (noise)

e.g.

Brownian noise

$$\sqrt{F_n^2} = \sqrt{4k_B T\, B\, \Delta f}$$

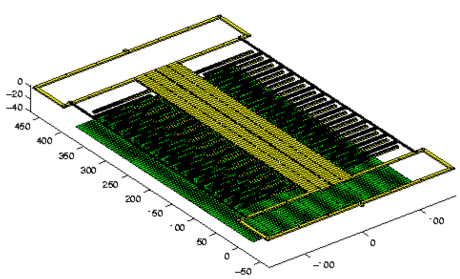


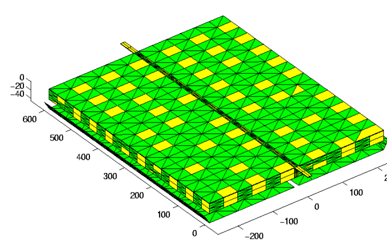
- Adverse interaction with Interface circuits ?
- Electromechanical feedback systems stable ?
- Design for manufacturability, testability
  - minimize sensitivity to variations
  - account for device calibration

c. Carnegie Mellon

Can we answer the design questions ?

- Develop a solid model of the geometry
- Mesh it
- Simulate via Finite Element/Boundary Element





Figures courtesy D. Ramaswamy and J. White, MIT (Transducers '99).

c. Carnegie Mellon

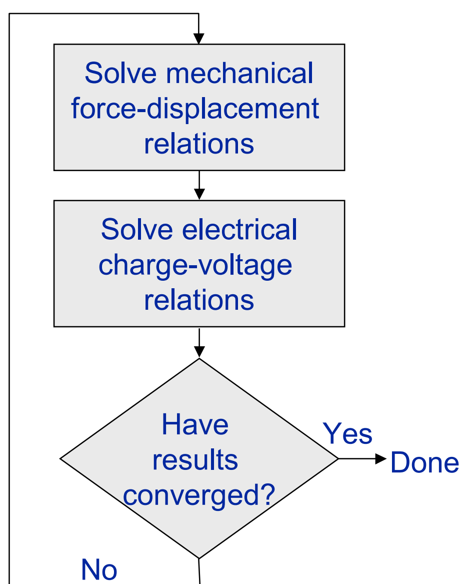
3-D Electrostatic and Elastostatic Solvers

- Electrostatics
  - Accelerated Boundary-Element Methods (FastCap derivatives)
  - Computes charge distribution given potentials
  - Analyzes whole comb drives in minutes
- Elastostatics
  - Nonlinear Finite Element Analysis
  - Computes structure deformation given applied pressure
- But,
  - Charge distribution applies pressure on structure
  - Structure deforms, altering the field,
  - Hence charge distribution changes

c. Carnegie Mellon

Coupled Electromechanical Solvers

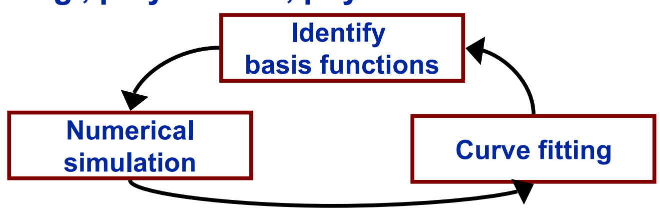
- Available from: ANSYS, CFDRC, Coventor, Intellisense, ...
  - Relaxation scheme with black-box solvers
  - Or, directly couple the solvers
- Can add more energy domains
  - e.g., thermal, fluidic



c. Carnegie Mellon

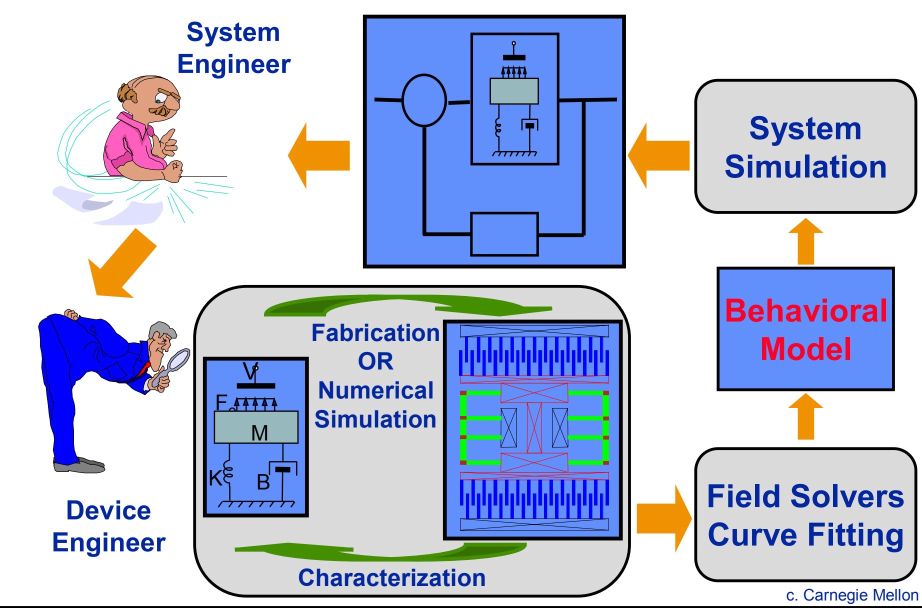
Behavioral Modeling ("Macromodeling")

- Low-level physics-based numerical simulation becomes impossible for large problems
  - Simulations are slow and memory intensive
  - Mixed-energy domains $\Rightarrow$ coupled simulation
- Solution is to partition problem
- Generate analytic equations (explicit equations or ODE's) for use in higher-level behavioral simulation
- Curve-fit using user-selected basis functions
  - e.g., polynomials, physics-based functions



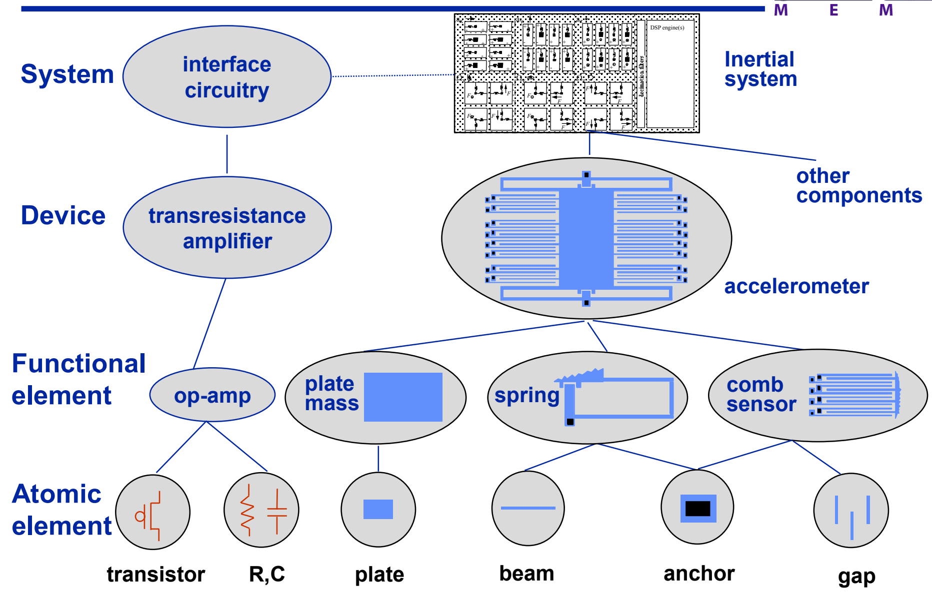
c. Carnegie Mellon

Bottom Up Design Methodology



c. Carnegie Mellon

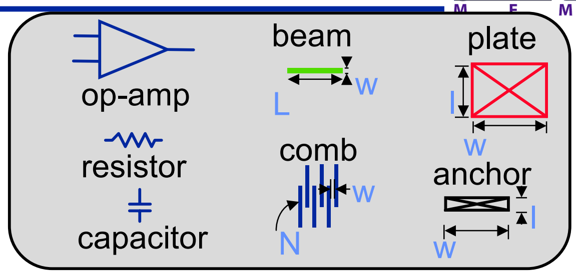
MEMS Design Hierarchy

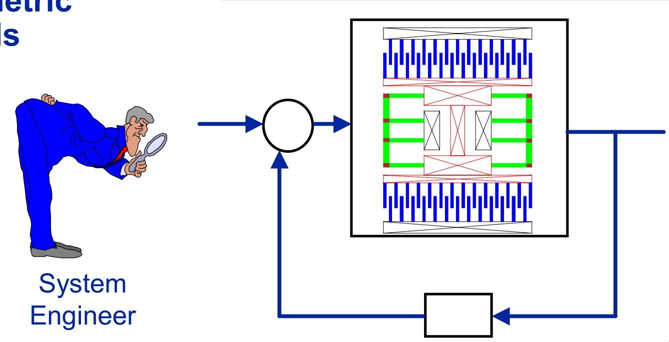


c. Carnegie Mellon

Top Down Design for MEMS

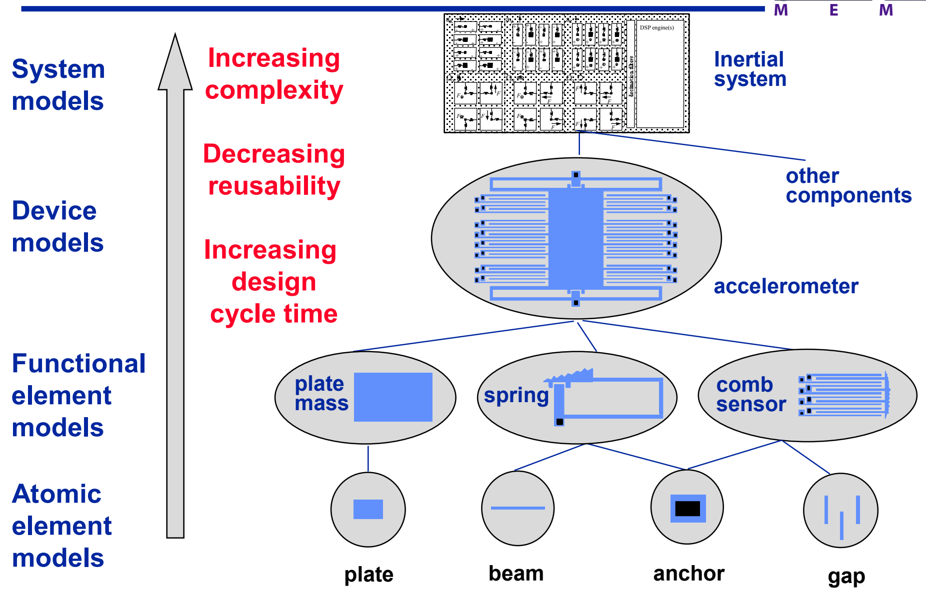
- Methodology for interoperability of models at all levels
- Emphasis on reusable, parametric models





c. Carnegie Mellon

MEMS Model Hierarchy



c. Carnegie Mellon

Outline

- MEMS Design Issues
- Process & Design Abstractions
- MEMS Circuit Level Modeling & Simulation
- Layout Generation
- Layout Verification
- Mesh Generation
- Synthesis
- Summary

c. Carnegie Mellon

Circuit-level Modeling

- Models must be
  - Accurate
  - Analytical or ODE representation (lumped)
  - Correct energy conservation and dissipation
  - Models static and dynamic behavior
  - Easy to connect to system-level simulators
- Analog HDLs encodes of models for simulation
- System designer wants design flexibility
  - Identify generally useful components
  - Parameterize components for reuse

c. Carnegie Mellon

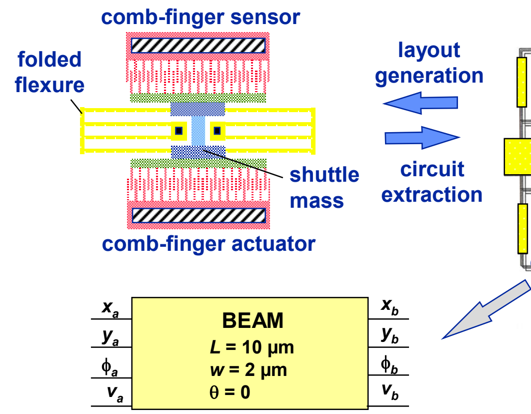
Prior/Current Efforts

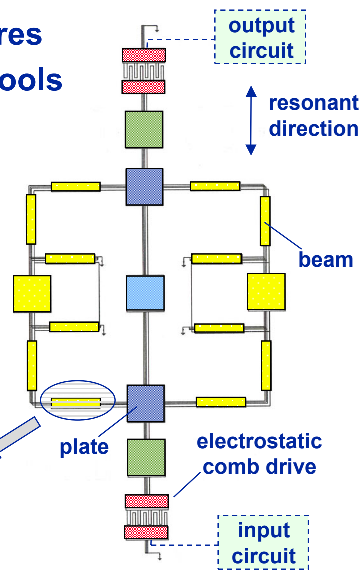
- NODAS – CMU
  - J. Vandemeer, et al., ASME IMECE’97
  - Licensed to Coventor and MEMSCAP
  - Models in MAST with simulation in Saber
  - Models in VerilogA with simulation in Cadence
- SUGAR – UC Berkeley
  - N. Zhou, et al., MSM’98
  - Models directly in matrices with simulation in Matlab
- ARCHITECT – Coventor
  - G. Lorenz, et al., MSM’98 (originally with R. Bosch)
  - Models in MAST with simulation in Saber
  - Models in VerilogA with simulation in Cadence
- MEMSMASTER – MEMSCAP
  - D. Mouliner, et al., DTIP’01
  - Models in VerilogA with simulation in Cadence
  - Models in Eldo with simulation in Mentor Graphics

c. Carnegie Mellon

Simulation Methodology in NODAS

- **Schematically compose structures**
- **Embedded in commercial EDA tools (Cadence, VerilogA)**





c. Carnegie Mellon

Behavioral Circuit Modeling

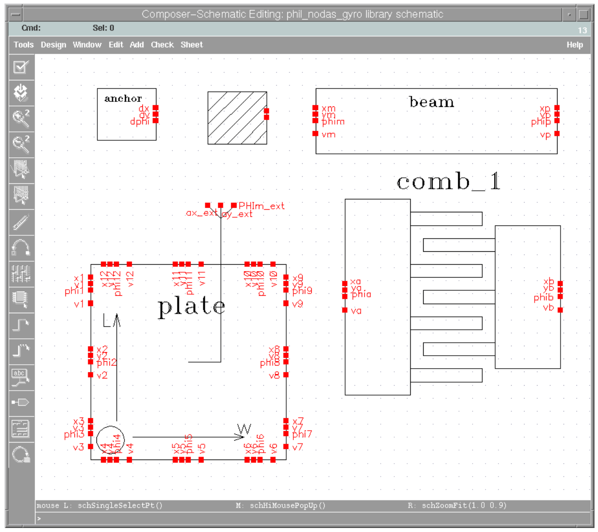
- **Models are coupled only through elements' I/O pins**
- ***e.g.,* beams and plates are modeled as lumped mass-spring-damper systems**

```
dy = cos_dc*Pos(yp,ym) - sin_dc*Pos(xp,xm);
F_yp = ms/420*(L*(13*1e6*Aphim-22*1e6*Aphip)
       + 54*Aym+156*Ayp)) + dampy*Vyp
       + 12*`E*Iz/(L*L*L)*(dy - 1e6/2*L*chip_phi);
Fchip_yp = F_yp*cos_dc + F_xp*sin_dc;
F(yp) <+ -Fchip_yp;
```

c. Carnegie Mellon

NODAS

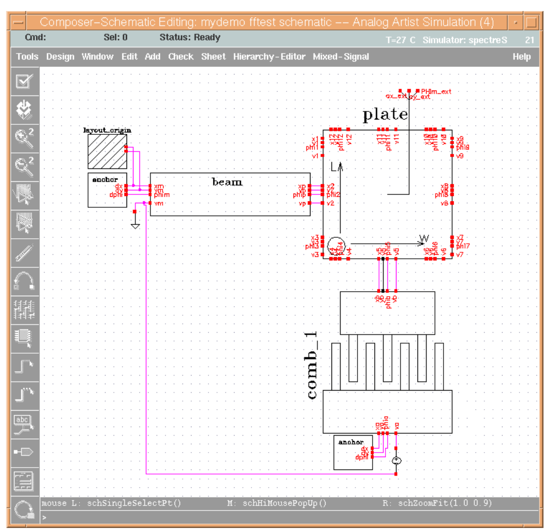
- **NOdal Design of Actuators & Sensors**
- **Elements (symbols and models) can be reused in new designs**



c. Carnegie Mellon

Simulation

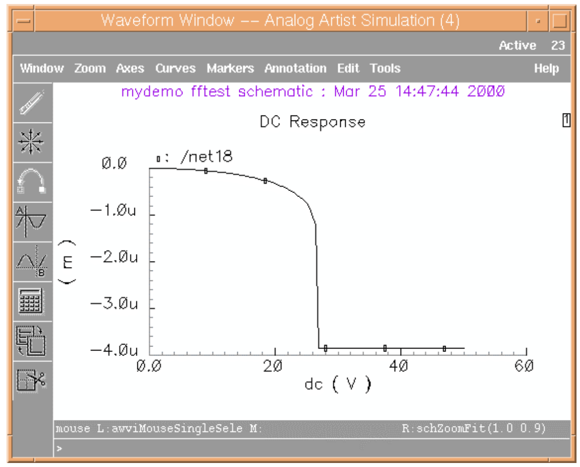
- **Behavioral simulation in Analog Artist, Spectre**



c. Carnegie Mellon

Simulation

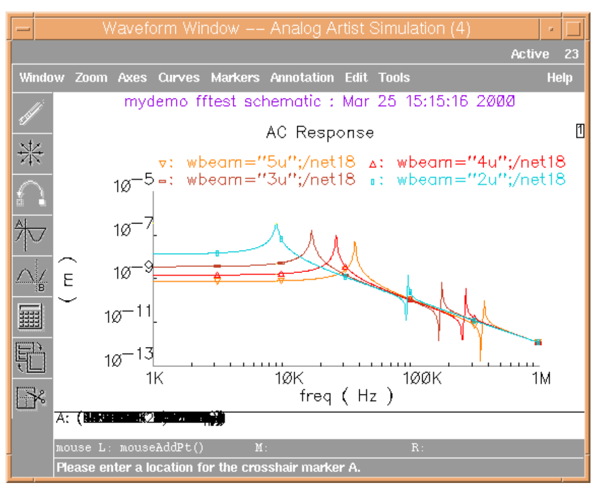
- Behavioral simulation in Analog Artist, Spectre
- All analysis modes available:
  - dc



c. Carnegie Mellon

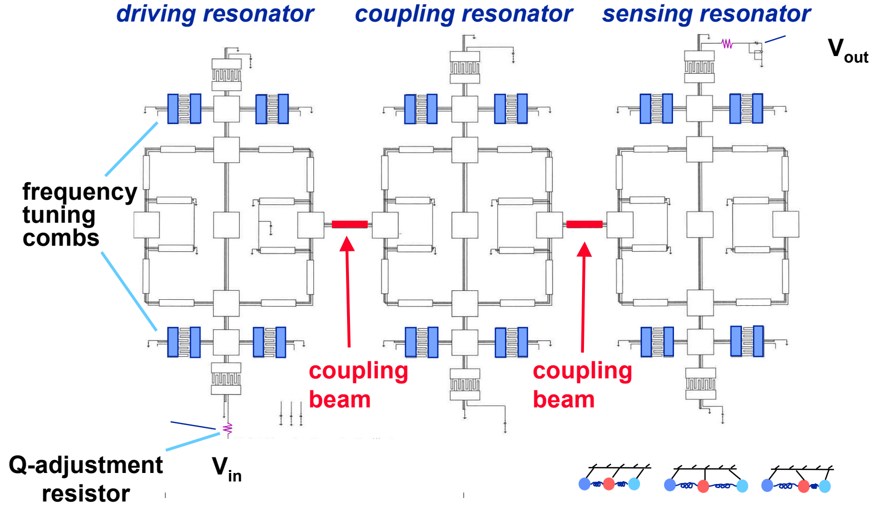
Simulation

- Behavioral simulation in Analog Artist, Spectre
- All analysis modes available:
  - dc
  - ac
  - parameter sweep
  - Monte-Carlo
  - transient

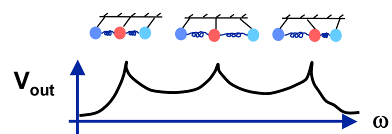


c. Carnegie Mellon

Mixed-Domain Design Example 1: MEMS Bandpass Filter



Principle of operation:

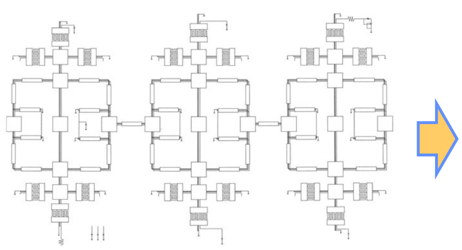


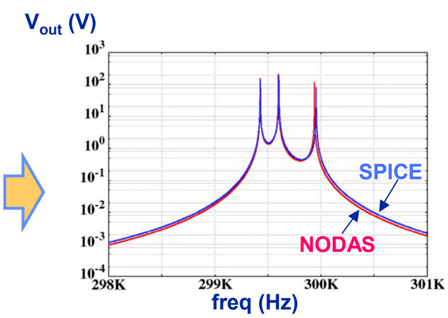
K. Wang *et al.*, MEMS 1997

c. Carnegie Mellon

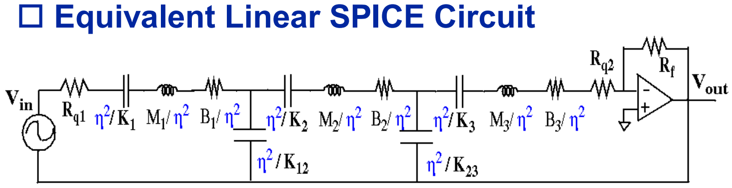
Mixed-Domain Design Example 1: Bandpass Filter Verification

- **NODAS MEMS Circuit**





- **Equivalent Linear SPICE Circuit**

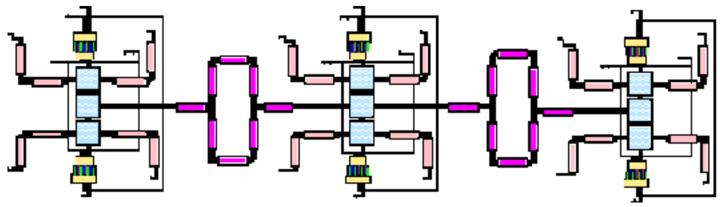


Q. Jing *et al.*, MEMS 2000

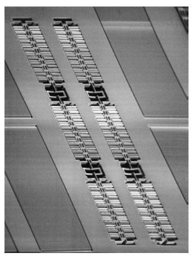
c. Carnegie Mellon

Mixed-Domain Design Example 1: CMOS-MEMS Bandpass Filter

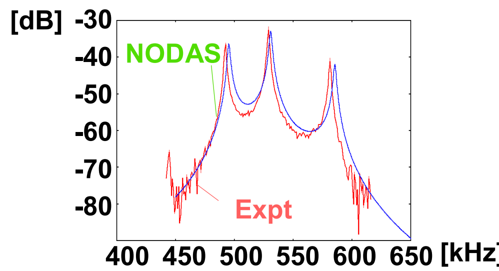
- NODAS Schematic



- SEM of fabricated device

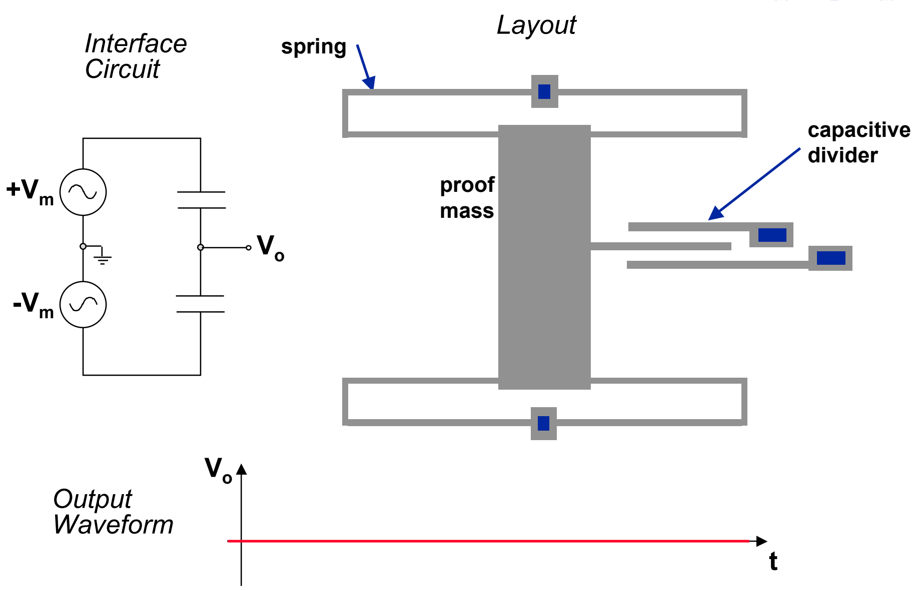


- NODAS vs. Experiment



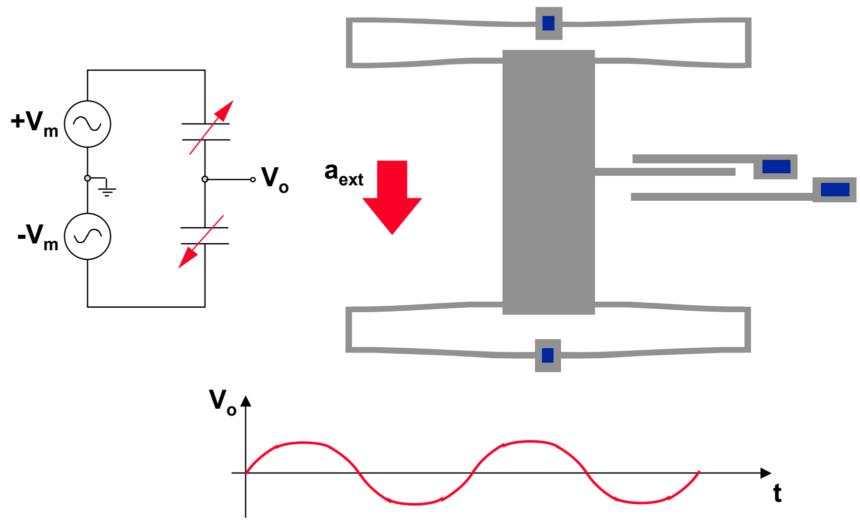
c. Carnegie Mellon

Capacitive Accelerometer Basics



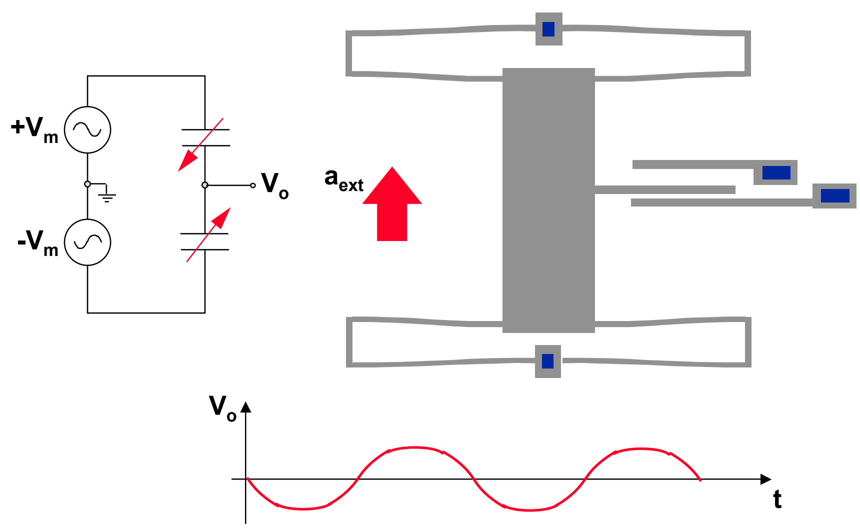
c. Carnegie Mellon

Capacitive Accelerometer Basics



c. Carnegie Mellon

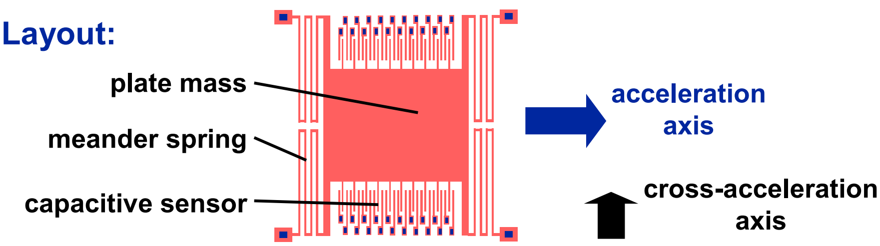
Capacitive Accelerometer Basics



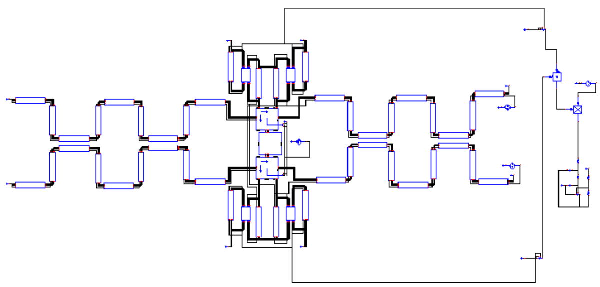
c. Carnegie Mellon

Mixed-Domain Design Example 2: Lateral Accelerometer

- **Layout:**



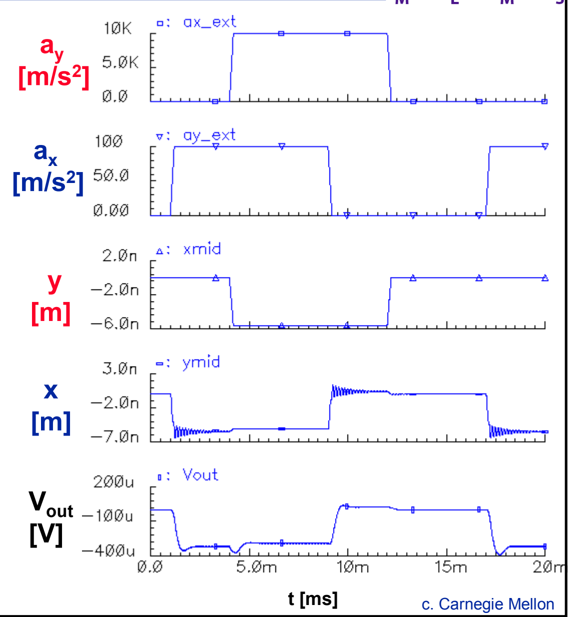
- **NODAS schematic:**



c. Carnegie Mellon

Mixed-Domain Design Example 2: Manufacturability Simulation

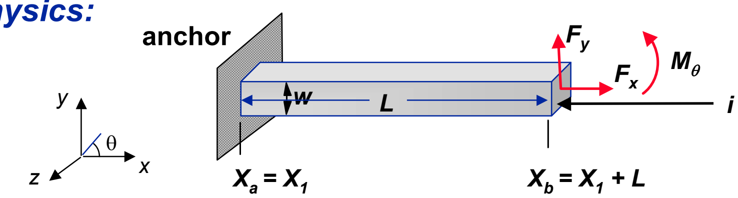
- **Identical beam widths:**
  - **cross-axis sensitivity = 0**
- **5% mismatch:**
  - **cross-axis sensitivity ~ 10^{-3}**
- **Transient analysis can be used to predict some failure modes**



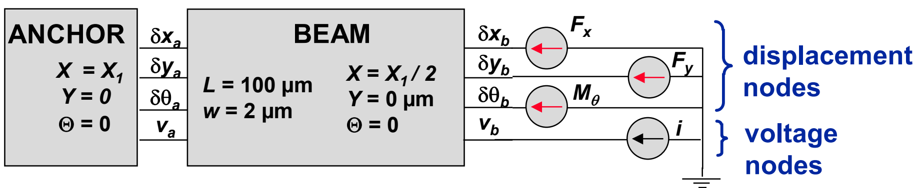
c. Carnegie Mellon

MEMS Circuit Representation: Cantilever Beam Example

Physics:



Circuit:



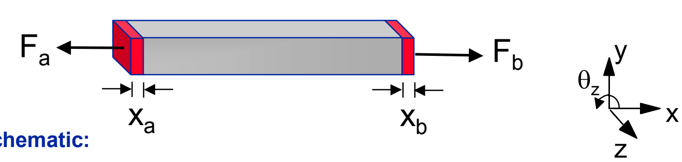
- Across variables: displacement, angle, voltage
- Through variables: force, moment, current
  - Branch relations: $\Sigma\ i = 0$; $\Sigma\ F = 0$; $\Sigma\ M = 0$

c. Carnegie Mellon

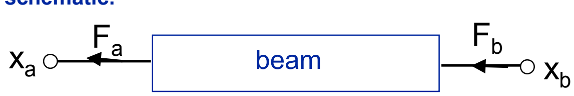
Nodal Conventions

- Across variables (x, y, θ_z displacement, voltage)
  - Positive valued displacements are in positive axial direction
  - Positive valued angles are counterclockwise around axis
- Through variables (F_x, F_y forces, M_z moment, current)
  - Force flowing into node acts in positive axial direction
  - Moment flowing into node acts counterclockwise around axis

Example: beam in tension



Equivalent schematic:



c. Carnegie Mellon

Behavioral Circuit Modeling

- Primary assumption is that element models are coupled only by nodes
- Beams and plates are modeled as mass-spring-damper systems driven at discrete positions corresponding to the nodes

$$[F] = [m]\,[\ddot{x}] + [B]\,[\dot{x}] + [k]\,[x]$$

$$[x] = [x_a \quad y_a \quad \theta_a \quad x_b \quad y_b \quad \theta_b]^T$$

- Electrostatic gaps are modeled as capacitors with moving electrodes

$$C = \varepsilon_0 A / g([x])$$

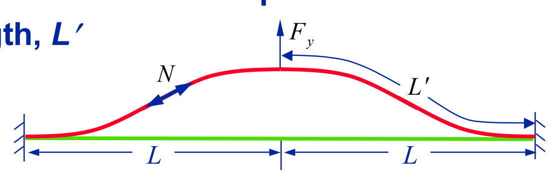
$$[F] = 0.5\, V^2\, [dC/d[x]]$$

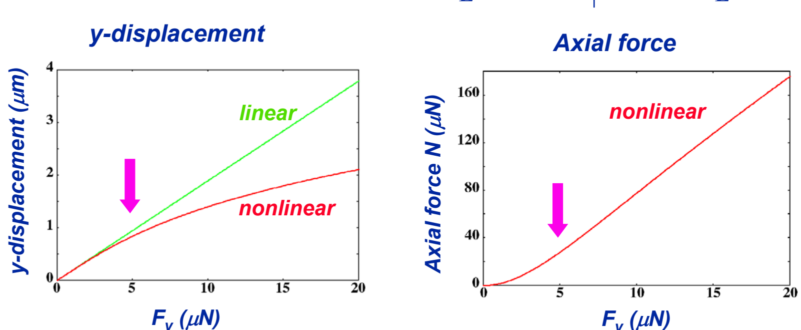
- Implemented in Analogy MAST/Saber and Cadence Verilog-AHDL/Spectre

c. Carnegie Mellon

Sources of Geometric Nonlinearity I: Large Axial Stress Stiffening

- Example: Fixed-fixed beam
- Beam nonlinearity starts at small displacement
- Effective beam length, *L′*
- Axial force, *N*

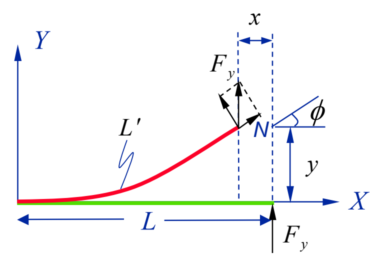




c. Carnegie Mellon

Sources of Geometric Nonlinearity II: Large Geometric Deflection

- Example: Cantilever beam
- Beam foreshortening, *x* and *y* are coupled
- Force projection into axial stress
- Cubic shape function valid only for small deflection
  - FEA: incremental loading & coordinate update
  - NODAS: coordinate transformation



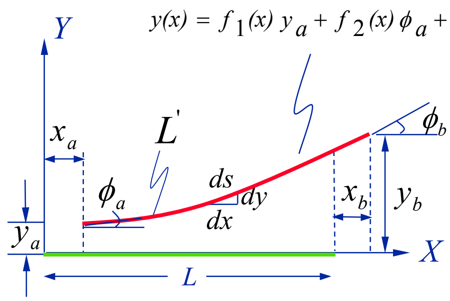
c. Carnegie Mellon

Effective Beam Length, L'

- Calculation of L' based on cubic-shape function

$$y(x) = f_1(x)\, y_a + f_2(x)\, \phi_a + f_3(x)\, y_b + f_4(x)\, \phi_b$$

f_i (x): cubic shape functions for small displacements



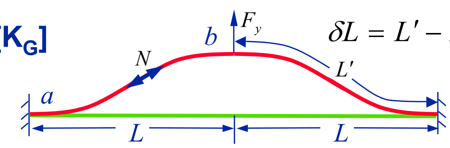
$$L' = \int ds = \int_{x_a}^{L+x_b-x_a} \sqrt{1 + \left(\frac{dy}{dx}\right)^2}\, dx$$

$$\delta L = L' - L$$

c. Carnegie Mellon

Axial Force, *N*

- **Geometric stiffness matrix, [K_G]**
- **Calculation of axial force, *N***



$$[F] = [K_0 + K_G(x)][x]$$

Linear stiffness matrix (K_0)

Geometric stiffness matrix ($K_G(x)$)

$$\overbrace{N(x) * [K_{G0}]} = \overbrace{\cancel{\frac{EA}{L}(x_a - x_b)}}^{N(x)} \overbrace{\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & * & * & 0 & * & * \\ 0 & * & * & 0 & * & * \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & * & * & 0 & * & * \\ 0 & * & * & 0 & * & * \end{bmatrix}}^{[K_{G0}]}$$

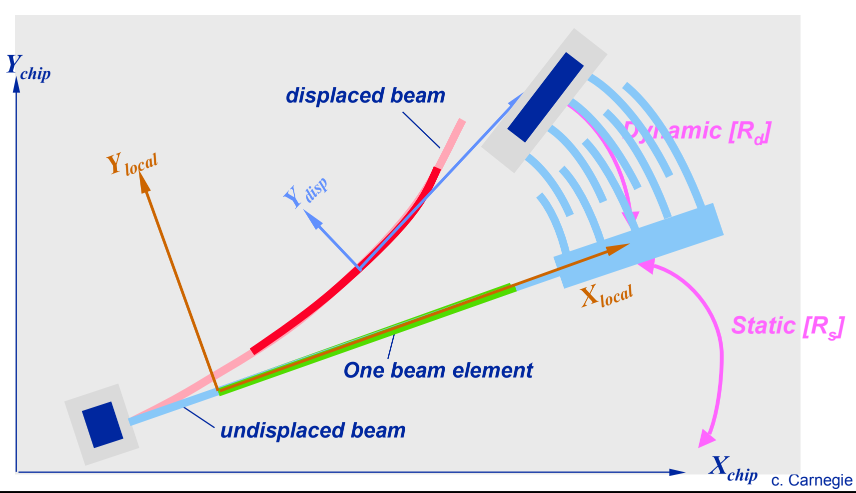
Modified to: $N = \frac{EA}{L}\delta L$

Ref: Przemieniecki, Theory of Matrix Structural Analysis, 1968

c. Carnegie Mellon

Coordinate Transformations

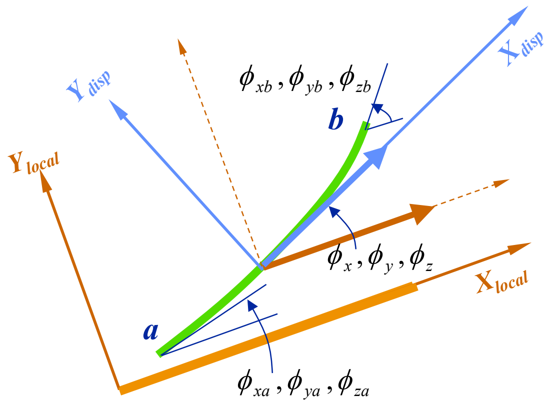
- **Chip frame: specifies layout position**
- **Local frame: specific to each element**
- **Displaced frame: shape functions are applied**



c. Carnegie Mellon

Dynamic Rotation

- Displacements in local frame are large
- Displacements in displaced frame are small
- Averaging rotations at node *a* and node *b*



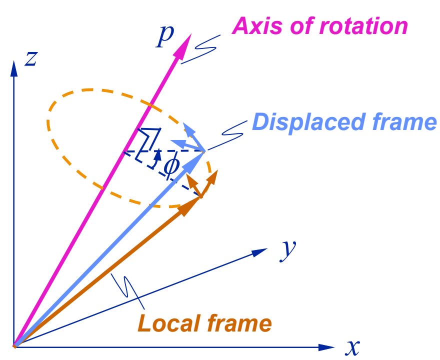
Rotation angles in local frame

$$\phi_x = (\phi_{xa} + \phi_{xb})/2$$
$$\phi_y = (\phi_{ya} + \phi_{yb})/2$$
$$\phi_z = (\phi_{za} + \phi_{zb})/2$$

c. Carnegie Mellon

Rotation About an Axis

- General, unique definition



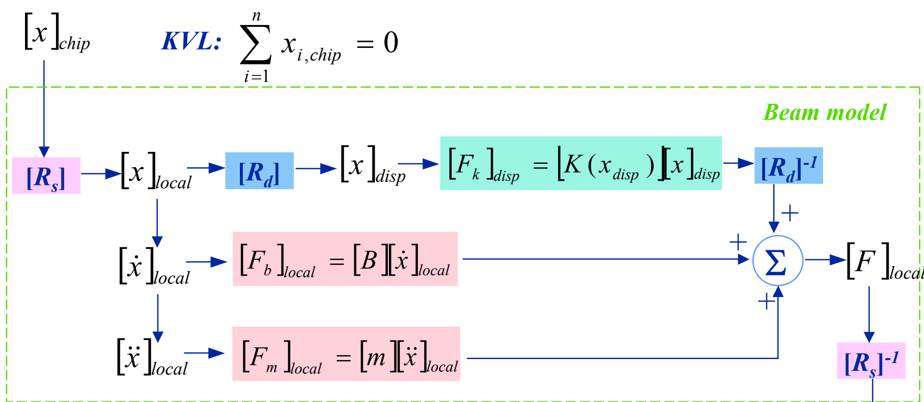
Used to form rotation matrix

$$\phi = \sqrt{\phi_x^2 + \phi_y^2 + \phi_z^2}$$
$$p_x = \phi_x / \phi$$
$$p_y = \phi_y / \phi$$
$$p_z = \phi_z / \phi$$

Ref: Glassner, Graphics Gems, 1990

c. Carnegie Mellon

Beam Model Structure



- In chip frame:
  - System matrix is built by the simulator (Spectre)
  - Self-consistent solution satisfying KCL and KVL is solved based on network topology

$[F]_{chip}$

KCL:

$$\sum_{i=1}^{m} F_{i,chip} = 0$$

c. Carnegie Mellon

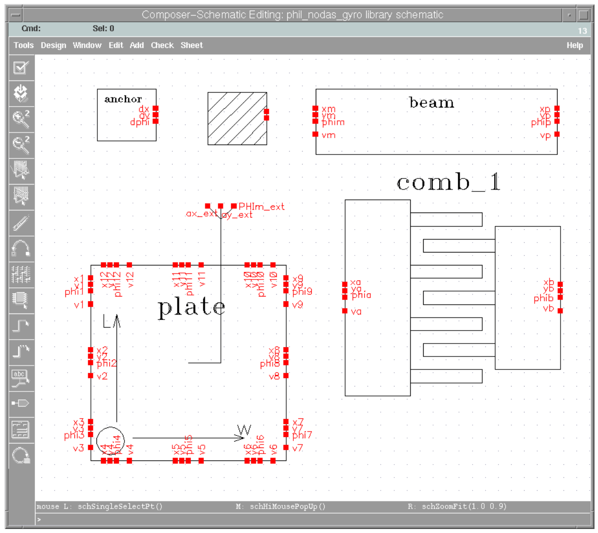
Outline

- MEMS Design Issues
- Process & Design Abstractions
- MEMS Circuit Level Modeling & Simulation
- Layout Generation
- Layout Verification
- Mesh Generation
- Synthesis
- Summary

c. Carnegie Mellon

Symbol Library

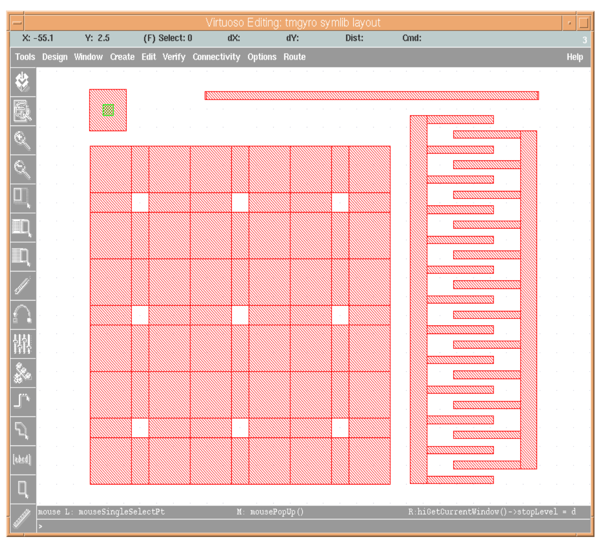
- **Low-level elements are:**
  - **Anchor**
  - **Beam**
  - **Plate**
  - **Gap**
  - **Comb**



c. Carnegie Mellon

Layout Generation

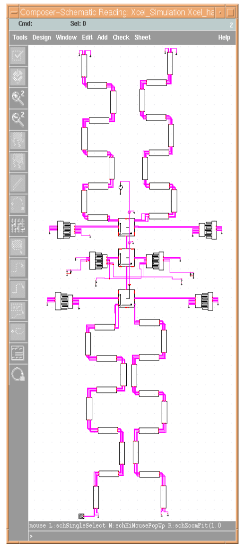
- **Automated layout is hierarchically p-cell (parameterized cell) driven directly from elements**

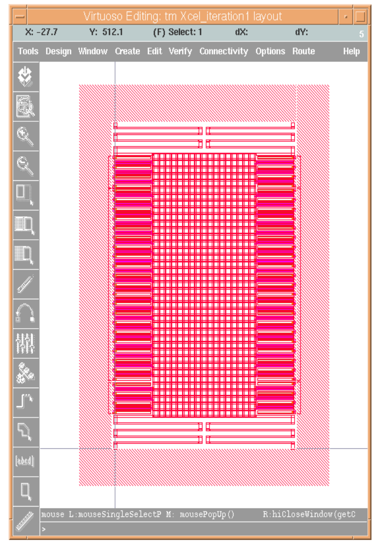


c. Carnegie Mellon

Layout Generation Example

- Connectivity derived from schematic

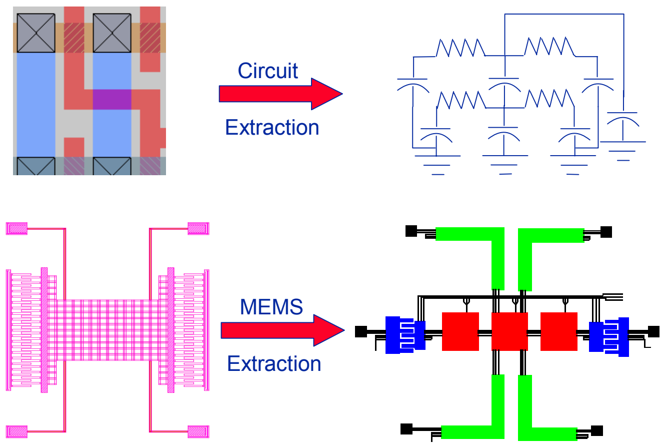




Outline

- MEMS Design Issues
- Process & Design Abstractions
- MEMS Circuit Level Modeling & Simulation
- Layout Generation
- Layout Verification
- Mesh Generation
- Synthesis
- Summary

MEMS Extraction for Layout Verification



- Recognizes layer overlaps and gaps
- Capacitors, resistors and transistors

- Recognizes layer overlaps, gaps and geometrical features
- Springs, plates, comb drives

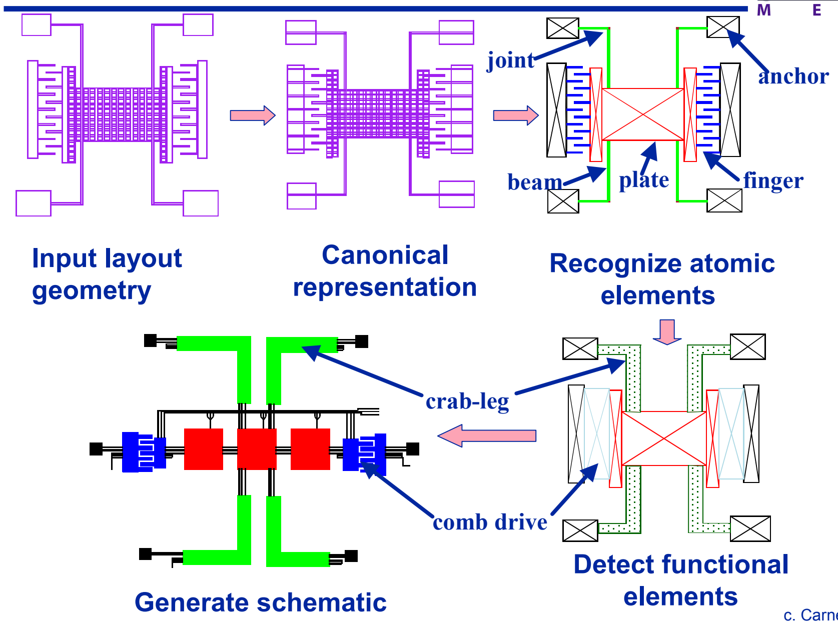
c. Carnegie Mellon

Previous Work

- N.R. Swart, *IEEE Design and Test of Computers*, vol.16, no. 19, pp. 39-47, 1999
  - Limited to hierarchical connectivity analysis
  - Verifies pin to pin connectivity of tagged layout
- Does not allow manual layout generation
- Fails to capture parasitics in the integrated layout

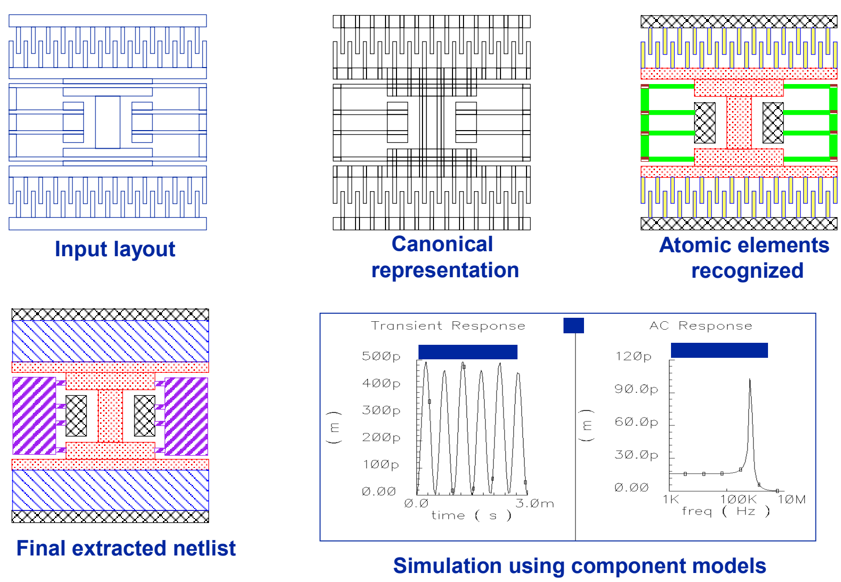
c. Carnegie Mellon

Extraction steps



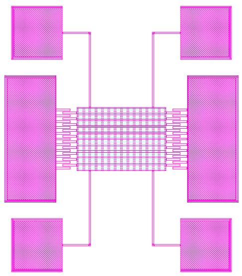
c. Carnegie Mellon

Eg: Folded Flexure Resonator



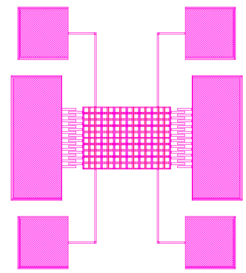
c. Carnegie Mellon

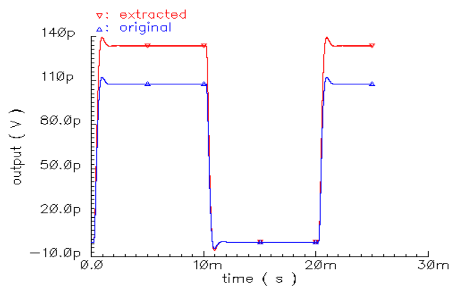
Effect of Mechanical Parasitics



layout from layout-generator

layout after putting in extra metal in plate

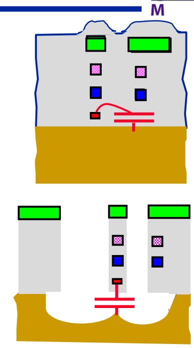


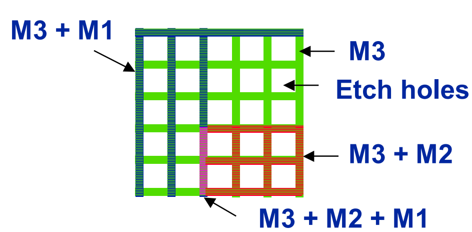


c. Carnegie Mellon

MEMS Parasitics

- Electrical
  - As in VLSI
- Electromechanical
  - Parasitic from released structure to substrate
- Mechanical
  - Metal routes cause additional mass
    - 43% holes, 57% m3, 34.2% m2, 35.91% m1

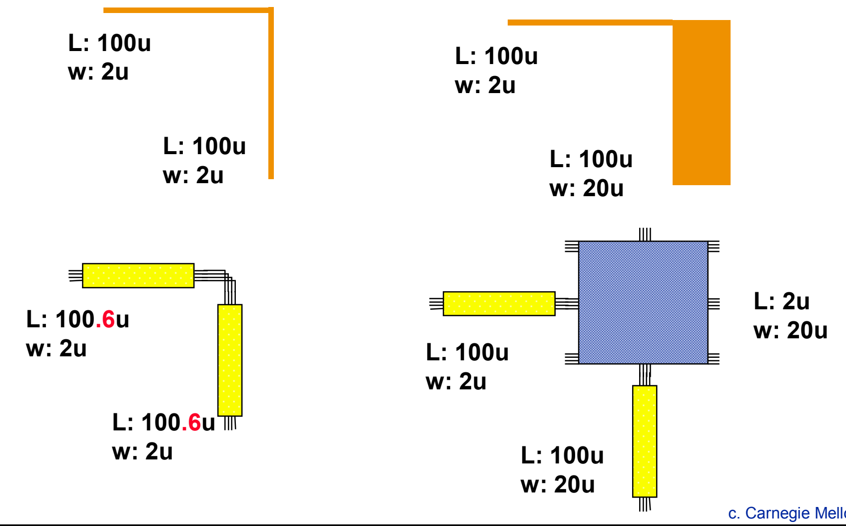




c. Carnegie Mellon

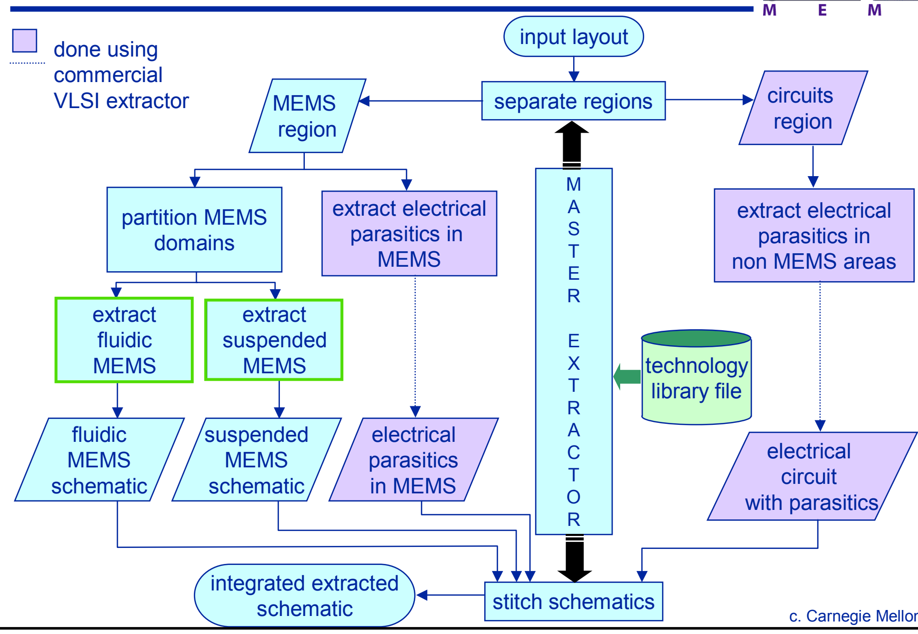
MEMS Parasitics

- **Mechanical**
  - **Joint between beams**



c. Carnegie Mellon

Extraction Flow



c. Carnegie Mellon

CMOS-MEMS Extraction

PROBLEMS | **SOLUTIONS**

Problem size larger

- multilayer structures
- etch holes
- $O(n^2)$ algorithms will be too slow

- hierarchical bin representation for storage
- scanline-based algorithms

More flexibility with electrical connectivity

- $O(n^2)$ connectivity algorithms will be too slow
- freedom to design complex types of springs and comb drives

- scanline connectivity algorithms of VLSI extractor
- graph-based algorithms
- user-defined library file with state-transition diagram

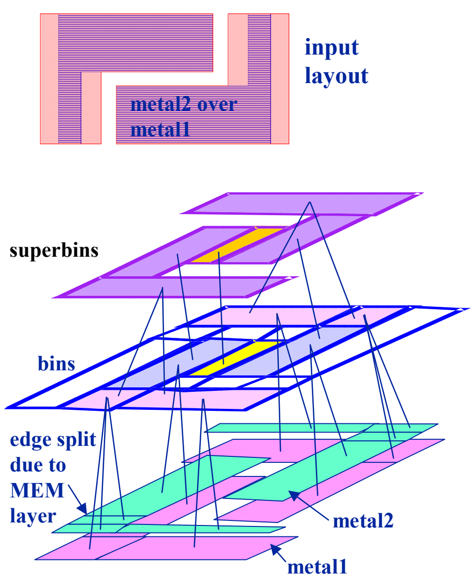
Mechanical and electrical parasitics

- parasitic mass and joints
- circuit parasitics
- parasitic capacitances effecting comb drive

- user-modifiable functions
- accurate parasitic calculation for MEMS areas
- integrated simulation

c. Carnegie Mellon

Hierarchical bin representation



- layers in canonical form
- merged layer (MEM layer) + gap layer form bins
- atomic recognition done on bins
- merged bins form superbins
- unrecognized empty bins discarded from superbins
- functional level recognition done on superbins

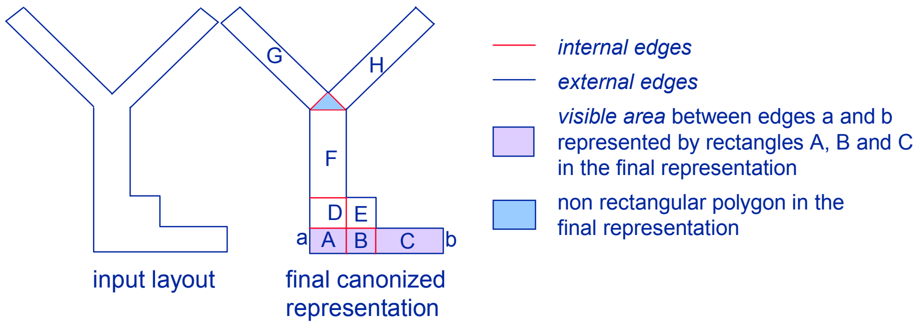
filled bin (plate)
filled bin (finger)
empty bin (gap)
empty bin (space)
filled superbin
empty superbin

B. Baidya *et al.*, MSM 2001

c. Carnegie Mellon

Canonical Representation

- Unique representation for any given layout geometry
- Minimum rectangles covering area between mutually visible parallel edges
  - Non Manhattan geometry will have rectangles and polygons
  - Manhattan geometry will have only rectangles
- Unique neighbor on each edge of resulting polygons and rectangles



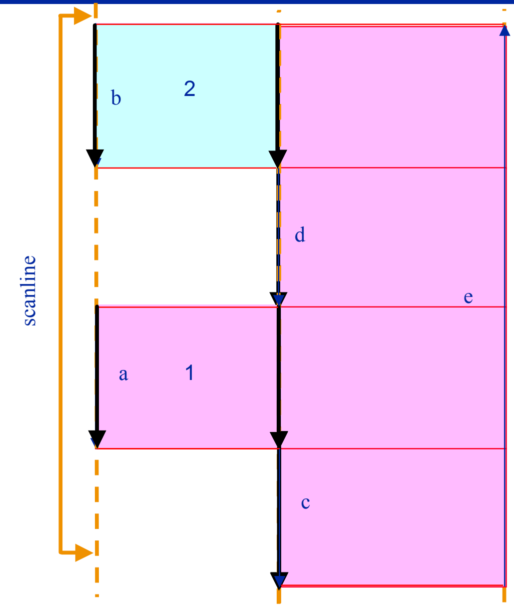
c. Carnegie Mellon

Canonization for Manhattan Geometry

- Simplification possible
  - Only two possible angles
  - Direction of edge can be used to predict its location
  - Final representation has only rectangles
- Only one scan
  - Using only vertical edges
  - Sorted w.r.t x coordinate, y coordinate and direction
- Scanline drags boxes associated with its edges
- New edge completes boxes that can be reached on scanline
  - Separate polygonization phase not required
- Simpler and faster than than the generalized algorithm
  - Time for creation of boxes = $O(n)$, n: final # of boxes
  - Time in operation = $O(e\lg m)$, e: # of edges, m: expected # of elements in scanline ~ $O(n^{0.5})$

c. Carnegie Mellon

Canonization Algorithm (Manhattan) : Example



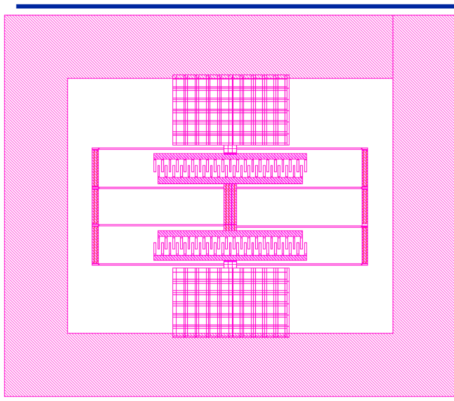
a,b inserted
c inserted
box 1 completed
box 2 dragged

d inserted
box 2 completed

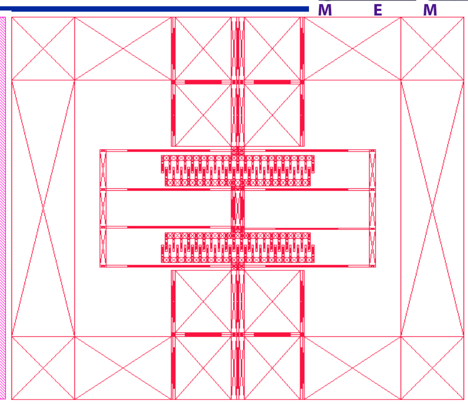
e inserted
all boxes completed

c. Carnegie Mellon

Canonization (Manhattan): Example



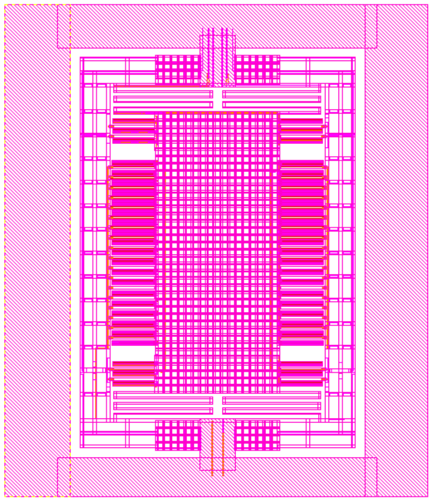
folded flexure resonator
(using only one structural layer)



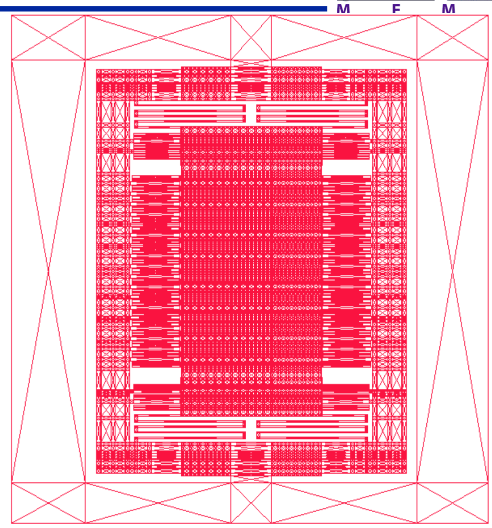
canonized layout
(>500 rectangles)

c. Carnegie Mellon

Canonization (Manhattan): Example



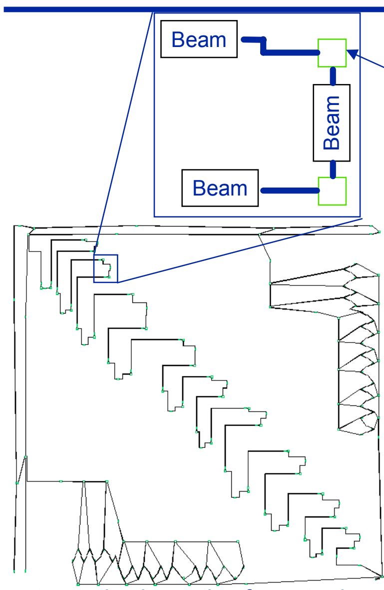
CMOS accelerometer
(3 metal layers)



canonized layout
(~50,000 rectangles)

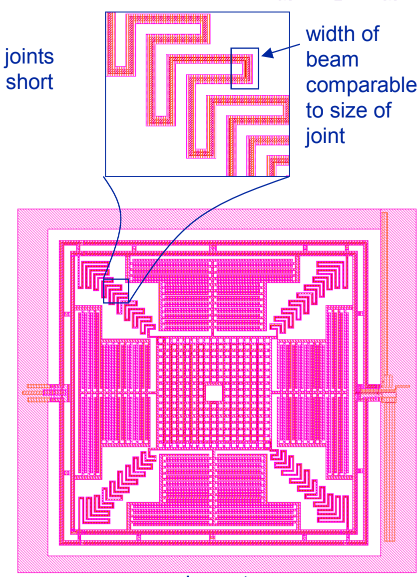
c. Carnegie Mellon

Z-accelerometer: Parasitic Joints



parasitic joints between short beam

extracted schematic of quarter layout

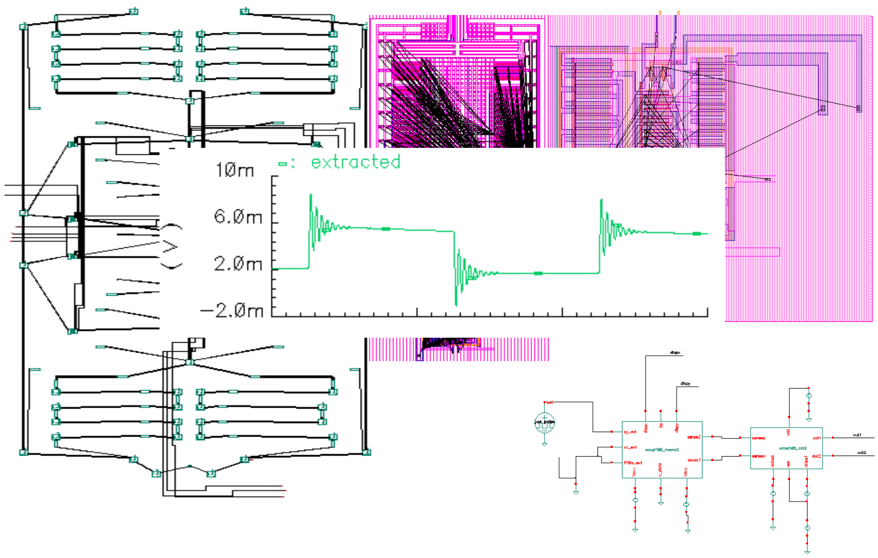


width of beam comparable to size of joint

layout

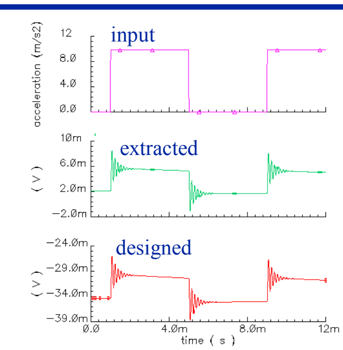
c. Carnegie Mellon

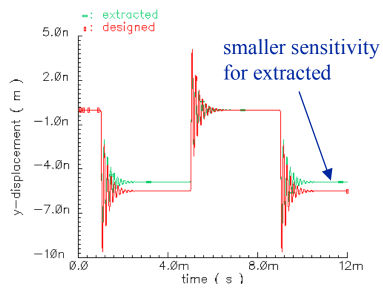
Example of Integrated Extraction: Accelerometer

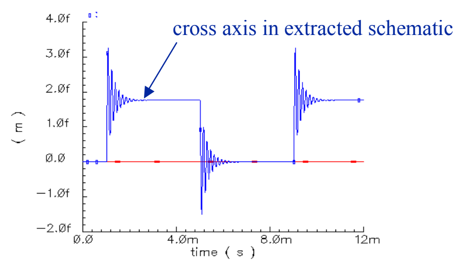


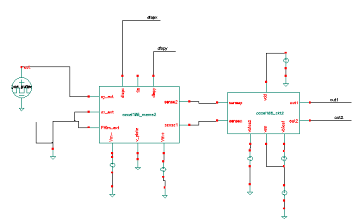
c. Carnegie Mellon

Example of Integrated Extraction: Accelerometer



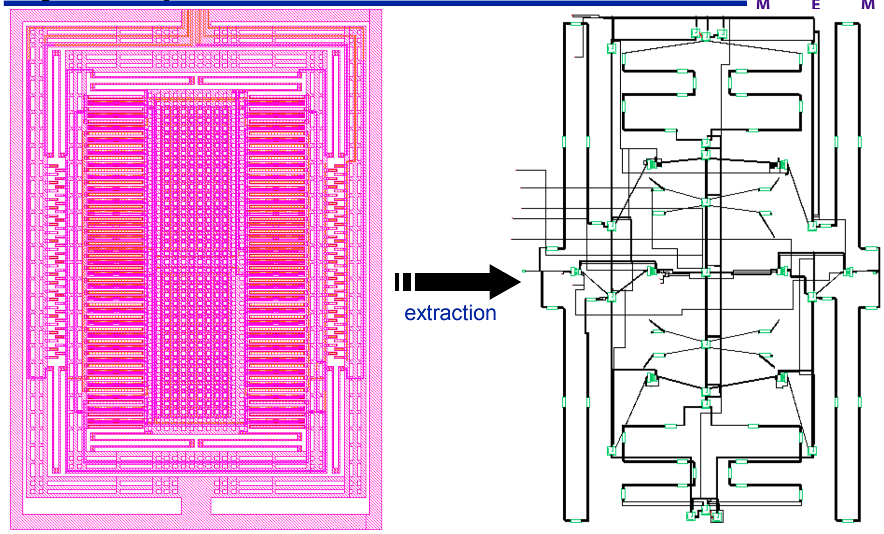






c. Carnegie Mellon

Example of Integrated Extraction: Gyroscope

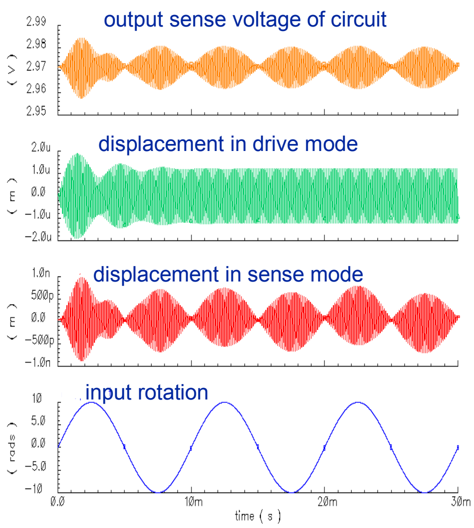


layout

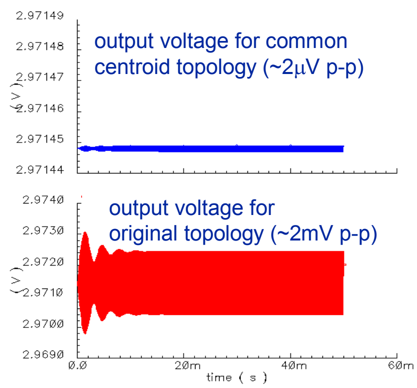
extracted schematic

c. Carnegie Mellon

Example of Integrated Extraction: Gyroscope

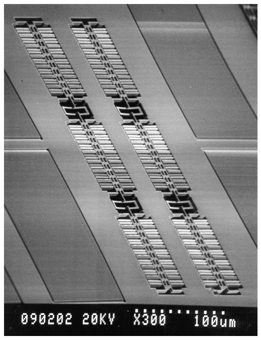


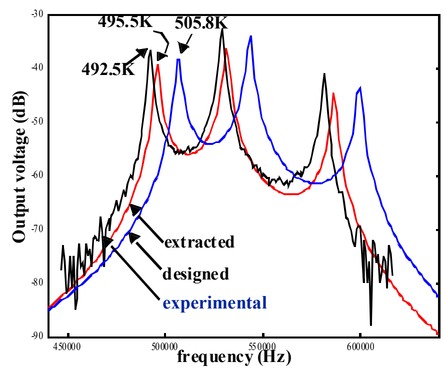
cross axis coupling at zero external rotation

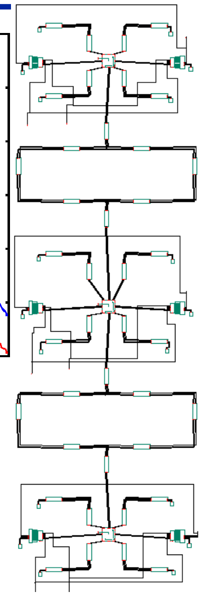


c. Carnegie Mellon

Example of Integrated Extraction: Filter





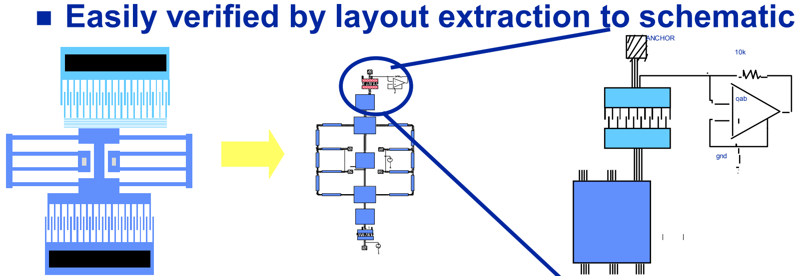


- Extracted schematic matches experimental results more than designed schematic

c. Carnegie Mellon

Context-Dependent Verification

- As in analog VLSI
  - Symmetry is extremely important in MEMS
  - Asymmetry induces mode coupling
    - Noise
    - Common Mode
- Manual interconnections can affect design
- What should be symmetric to what ?
  - Easily verified by layout extraction to schematic



c. Carnegie Mellon

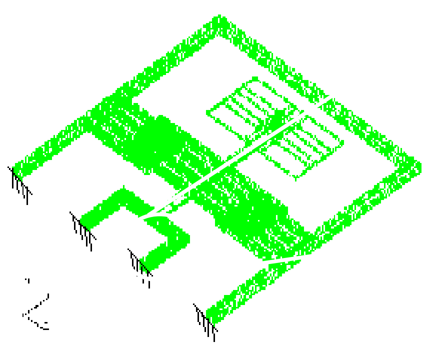
Outline

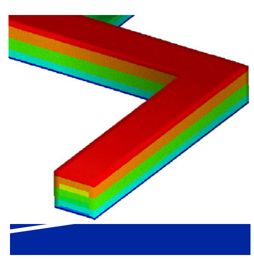
- MEMS Design Issues
- Process & Design Abstractions
- MEMS Circuit Level Modeling & Simulation
- Layout Generation
- Layout Verification
- Mesh Generation
- Synthesis
- Summary

c. Carnegie Mellon

Intelligent Mesh Generation

- Canonical Representation ⇔ minimal mesh
- Multi-layer CMOS-MEMS mesh generator
  - Recognizes beams, plates, and meshes appropriately

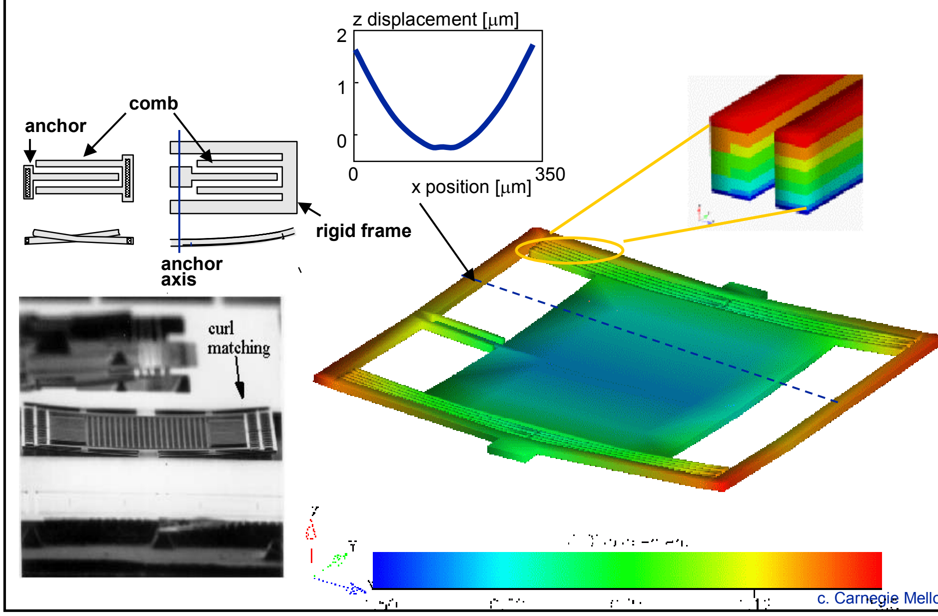




e.g., electrothermal actuator

c. Carnegie Mellon

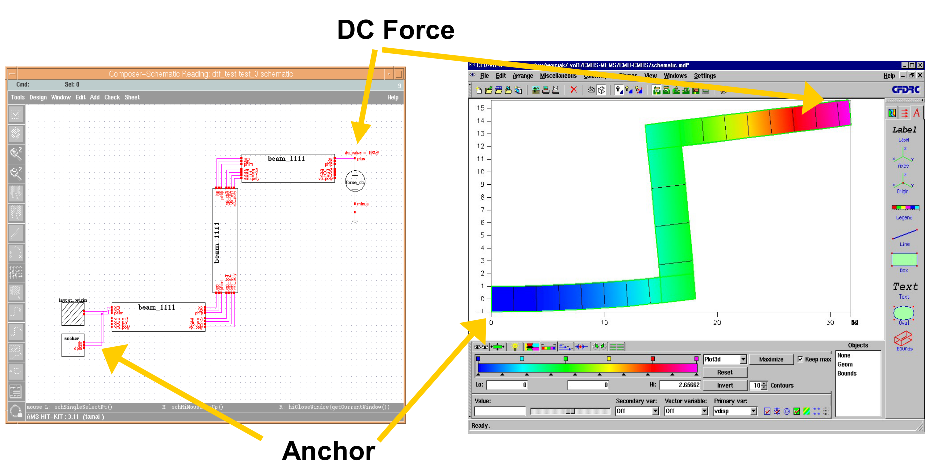
Curl in CMOS Accelerometer



c. Carnegie Mellon

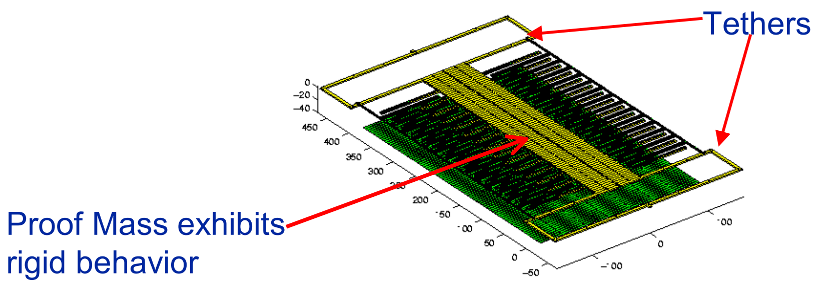
Schematic-Driven Mesh

- Integrates Schematic-To-Layout with Layout-To-Mesh
  - Schematic Source elements become Boundary Conditions



c. Carnegie Mellon

Rigid Elements in MEMS

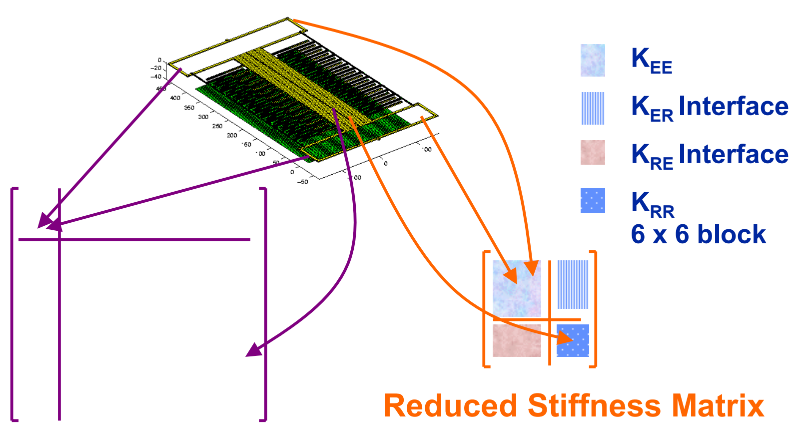


- Treat bulk as a Rigid Body with only 6 degrees of freedom, 3 Euler angles of rotation and 3 displacement variables

Figures courtesy D. Ramaswamy and J. White, MIT (Transducers '99).

c. Carnegie Mellon

Rigid Elastic Formulation



Figures courtesy D. Ramaswamy and J. White, MIT (Transducers '99).

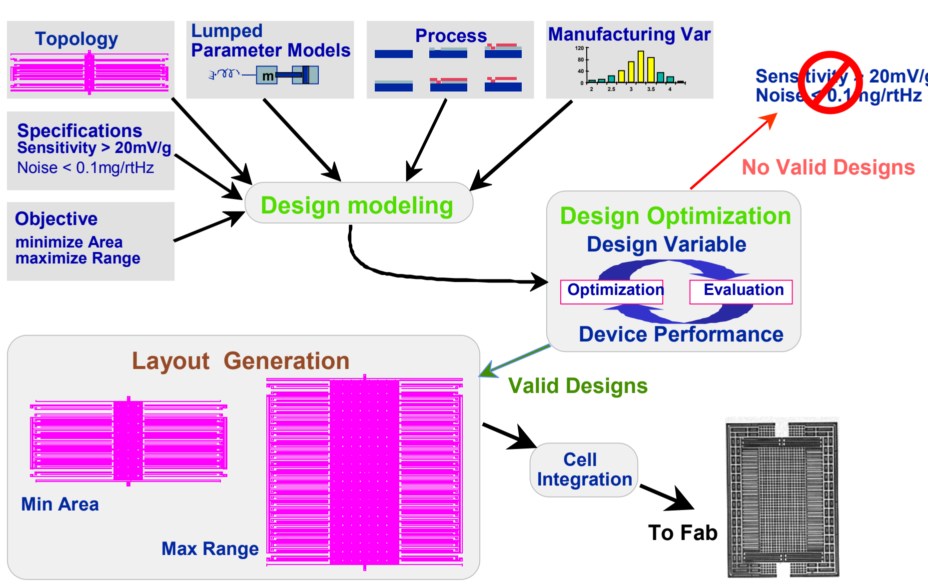
c. Carnegie Mellon

Outline

- MEMS Design Issues
- Process & Design Abstractions
- MEMS Circuit Level Modeling & Simulation
- Layout Generation
- Layout Verification
- Mesh Generation
- Synthesis
- Summary

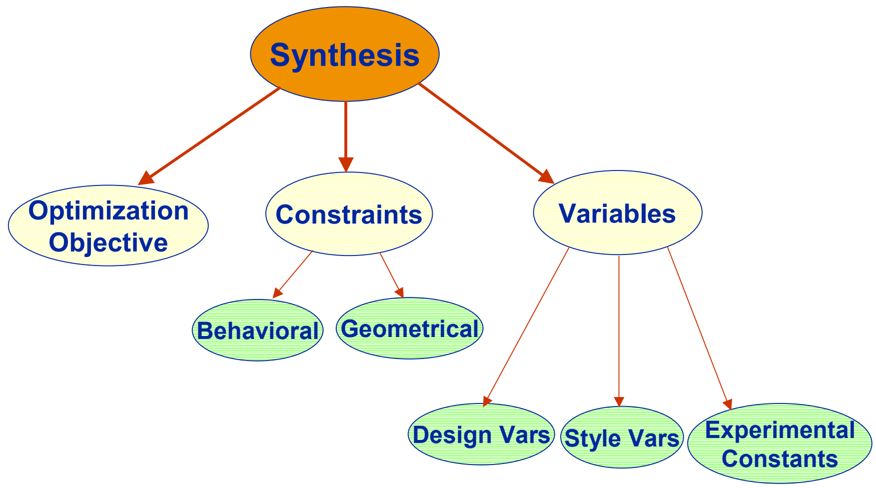
c. Carnegie Mellon

Optimization-based Synthesis



c. Carnegie Mellon

Synthesis Approach



c. Carnegie Mellon

Synthesis/Optimization Algorithm

Optimization Problem:

$$\underset{X \in \Re^n}{minimize} \quad \textbf{objective\_function}(X)$$

$$subject\ to \quad l \le \begin{Bmatrix} X \\ A_{linear} X \\ c_{non-linear}(X) \end{Bmatrix} \le u$$

Optimization Strategy:

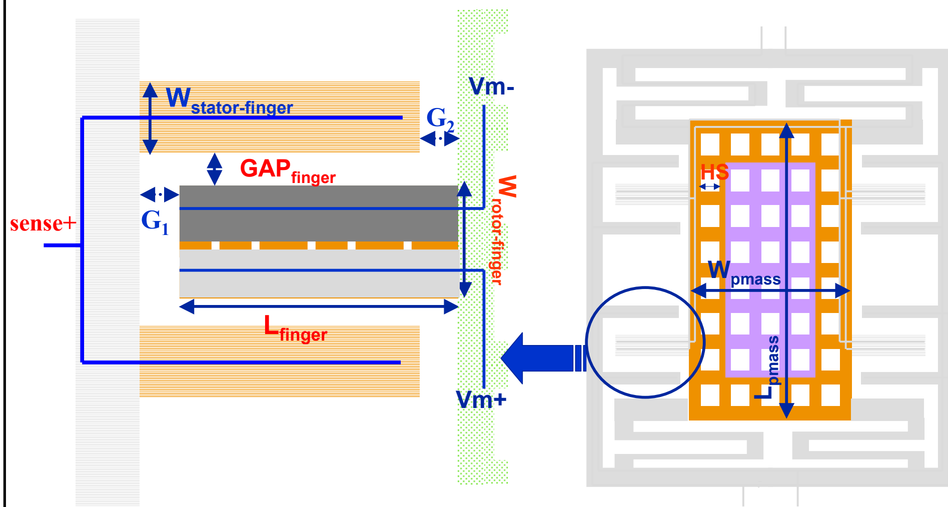
gradient based constrained non-linear optimization

Uses:

» **Multiple grid point sampling for initial start-point**
» **Sequential Quadratic Programming (*Lagrange-Newton Method*)**
» **Branch and Bound for integer valued variables**

c. Carnegie Mellon

Variables: Plate-mass/Comb-drive



c. Carnegie Mellon

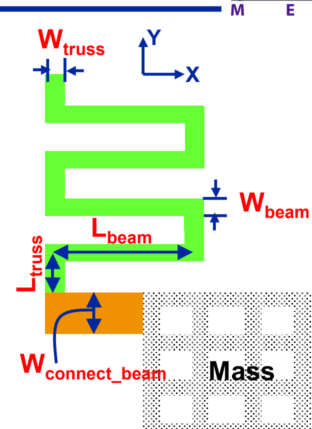
Variables: Spring

Low Cross-axis Sensitivity ⇒
spring symmetry (*w.r.t. x* axis)

Symmetry ⇒ #(truss beams) = ODD

⇒ Use a Thick Connecting Beam

⇒ Constraint: $K_{\text{connect beam}} \geq 10^{*}K_{\text{spring}}$



c. Carnegie Mellon

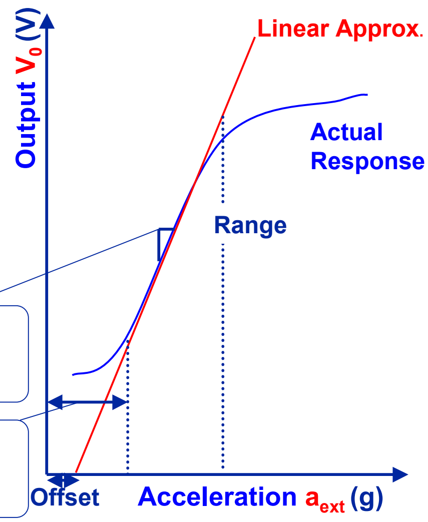
Synthesis: Functional Constraints

- Sensitivity (*slope*) > *spec*
- Noise (*resolution*) < *spec*
- Offset ~ *0*
- Range > *spec*
- Cross-axis sensitivity < *spec*
- Bandwidth > *spec*

- $\omega_{\text{(non-major axis)}} > 2\omega_{\text{(major-axis)}}$
- $\omega_{\text{(comb-finger)}} < \omega_{\text{(modulation voltage)}}/1.5$

Sens = $\dfrac{(C_1^{\,0}+C_2^{\,0})}{C_1^{\,0}+C_2^{\,0}+C_{para}}\,\dfrac{m}{k_x g_0}V_m$

Noise = $\sqrt{\left(\dfrac{\sqrt{4k_bTB}}{m}\right)^2+\left(\dfrac{v_{noise-ckt}}{Sens}\right)^2}$

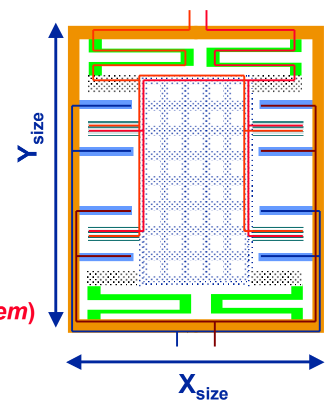


c. Carnegie Mellon

Synthesis: continued

Geometrical Constraints

- Area restrictions
  ($2*L_{finger} + W_{pmass} < X_{size} < 270\ \mu m$)
- Process design rules
  (minimum M3 gap = 0.9 μm)
- Relative size constraints
  (*e.g., all comb-units must fit on the plate-mass*)
- Gap constraints for mechanical release
  (*thicker structures need more space around them*)



Optimization Objectives

- Minimize Noise
- Maximize Sensitivity
- Minimize Area

c. Carnegie Mellon

Synthesis *vs. Manual Design*

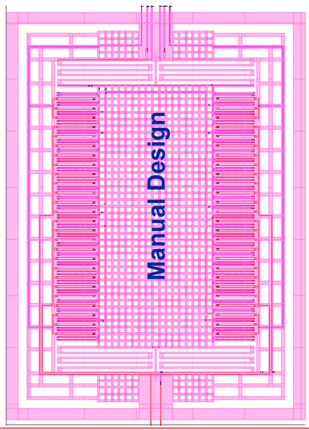
Specifications:

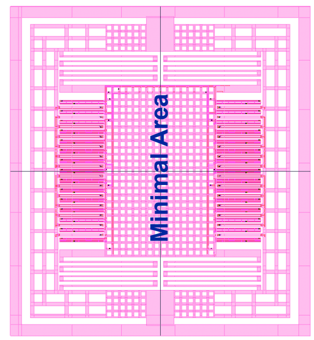
Sensitivity = 0.5 mV/G

Noise ≤ 83 μG/rtHz

Area ≤ 270x500 (μm)^2

Optimizes spring design to obtain same sensitivity with less mass & area





Spring Constant	1.56 N/m	0.63 N/m
Mass	0.56 μg	0.38 μg
Gap	1.5 μm	1.65 μm
Area (used)	100%	79%

c. Carnegie Mellon

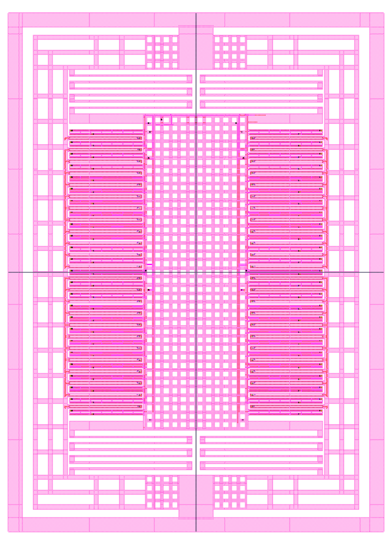
Synthesis: *Maximal Sensitivity*

	Spec	Obtd
Sensitivity(mV/G)	>0.5	1.97
Range (G)	>50	70
Noise (μG/rtHz)	<100	100
Area ((μm)^2)	<270x500	100%

Gap = 1.5 μm ***(= min value)***

w_o = 5 kHz

Limited by area specification



c. Carnegie Mellon

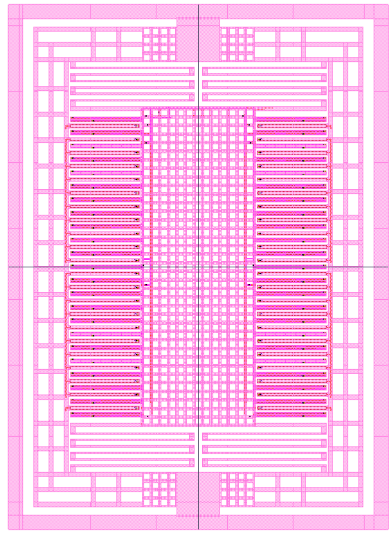
Synthesis: *Minimal Noise Objective*

	Spec	Obtd
Sensitivity(mV/G)	>0.5	0.5
Range (G)	>50	150
Noise (μG/rtHz)	<100	50
Area ((μm)^2)	<270x500	100%

Gap = 2.6 μm *(min value is 1.5 μm)*

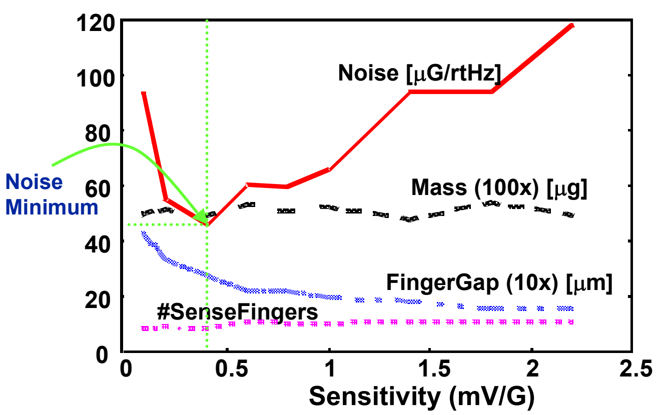
⇒ Squeeze film damping dominant over other forms of damping

Limited by sensitivity specification



c. Carnegie Mellon

Sensitivity *vs.* Noise *Trade-off Analysis*



Noise =

$$\sqrt{\left(\frac{\sqrt{4k_b TB}}{m}\right)^2 + \left(\frac{v_{noise-ckt}}{Sens}\right)^2}$$

To right of minimum:
FingerGap ↓ ⇒ Damping ↑ ⇒ Mechanical Noise ↑

To left of minimum:
FingerGap ↑ ⇒ Mechanical Noise ↓, Also Sensitivity ↓ ⇒ Electrical Noise ↑

c. Carnegie Mellon

More MEMS CAD Needs

- Answering additional questions
  - Noise
  - Thermomechanical drift
  - Stress
  - Manufacturing defects
- Design application areas with new physics
  - Optical manipulation
    - Optical
  - Biochemical systems
    - Chemical
    - Fluidic

c. Carnegie Mellon

Conclusions

- Multi-view, multi-level, multi-physics, multi-process design methodology
  - Ability to handle increased complexity
  - Increase in design reuse
  - Decrease in time to working designs
  - Reduction in design errors

⇒ Reduce the Design Productivity Gap

- Need
  - Systematic method for process parameter extraction
  - Designer Education

c. Carnegie Mellon

Acknowledgements

- Prof. Gary Fedder
- Several Students & Staff at Carnegie Mellon MEMS Lab
  - B. Baidya, V. Gupta, K. He, S. Iyer, Q. Jing, H. Lakdawala, S. Vemuri, W. Wojciak

- Funding
  - DARPA Composite CAD & MEMS Programs
  - National Science Foundation

c. Carnegie Mellon