System-Level Modeling and Design of Integrated MEMS

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System Design Bottleneck

- Increasing gap between technology advancement and ability to design new systems [SIA]
- Design team sizes need to increase to eliminate gap
MEMS Design Bottleneck?

- Same bottleneck, different scale
- How do we get design productivity to increase, so complexity can increase?

Outline

- MEMS Design Issues
- Process & Design Abstractions
- MEMS Circuit Level Modeling & Simulation
- Layout Generation
- Layout Verification
- Mesh Generation
- Synthesis
- Summary
Today’s MEMS Designers

- Process flow
- Materials characterization

1) Process design

- Modeling of physical interactions
- Layout-based design
- Interface circuits

2) Component design
Bottom-Up Design

Device design

System design

Macromodel Generation

Top-Down Design

fabrication requests

Foundry

Application-Specific Design

- Reusable, parametric models
- Macromodel bottleneck moved to library creation, and removed from design iteration

design rules, material parameters, device models
MEMS Design Issues

- Layout
  - Will it release?
  - Will it function?
  - Will it meet specifications?
    - Dynamic range
    - Sensitivity (parasitics)
    - Sensor resolution (noise)

- Design
  - Interface circuits
  - Electromechanical feedback systems
  - Device matching
  - Design for manufacturability, testability
    - minimize sensitivity to variations
    - account for device calibration

➤ Requires hierarchical design methodology

Integrated MEMS Design

- Application Driven ⇒ Low-volume custom MEMS

- Design Methodology Characteristics
  - Support wide variety of MEMS fab processes
  - Supporting a wide class of MEMS designs
  - Extensible to new MEMS design concepts
  - Fits into the existing VLSI design flows
  - Capable of evaluating integrated system designs
Outline

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Process Abstractions: CMOS Micromachining
Process Abstractions: Polysilicon Micromachining

- movable polysilicon beam
- anchored electrodes
- insulating plane
- ~ 2-3 µm
- > 2 µm

Process Abstractions: Technology Capture

- Decoupling of process complexity and design complexity through process abstraction
- MEMS processing derived from VLSI
- Use VLSI process abstractions
  - Layout technology file
  - Model technology file
  - Design rule file
  - Layout (parasitic) extraction file
Process Abstractions:
Layout Technology File

- Same as VLSI
- Interface to foundry
- Layer definition
  - GDS number
- Layer order
- Not required for simulation

```
(("Nwell" "drawing") 42 0 t)
(("Active" "drawing") 43 0 t)
...
(("Poly1" "drawing") 46 0 t)
(("P1Con" "drawing") 47 0 t)
(("Metal1" "drawing") 49 0 t)
(("Metal2" "drawing") 51 0 t)
```

```
(("POLY0" "drawing") 13 0 t)
(("HOLE0" "drawing") 41 0 t)
(("POLY1" "drawing") 45 0 t)
(("ANCHOR1" "drawing") 43 0 t)
(("HOLE1" "drawing") 44 0 t)
(("POLY2" "drawing") 49 0 t)
(("HOLE2" "drawing") 46 0 t)
```

Process Abstractions:
Model Technology File

- Process-dependent information
  - Layer thicknesses
  - Material properties
- Parameters common to all models in element library

```
`define m1_resistivity 0.07
`define m1_thickness 0.7u
`define m1_density 2700
`define spacer_gap 20u
`define E 62G
`define stress 300M
`define stress_gradient 10M
```

```
`define poly1_resistivity 10
`define poly1_thickness 2u
`define poly1_density 2330
`define spacer_gap 2u
`define E 165G
`define stress 3M
`define stress_gradient 0.1M
```
Process Abstractions:
Design Rule Check

- MEMS introduces
  - Sacrificial etch to release structure
- Microstructure release of depends on
  - Gap size
  - Gap shape
  - Gap spatial distribution

unreleased beam
unreleased plate
released plate

Process Abstractions:
MEMS-Specific Design Rules

- MEMS release step adds new constraints on design rules

- CMOS-MEMS Example:
  A – Minimum and maximum structural width
MEMS release step adds new constraints on design rules

CMOS-MEMS Example:
- A – Minimum and maximum structural width
- B – Minimum gap between structures
- C – Minimum structural metal extension
Process Abstractions: MEMS-Specific Design Rules

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  - A – Minimum and maximum structural width
  - B – Minimum gap between structures
  - C – Minimum structural metal extension
  - D – Minimum polysilicon spacing from edge

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  - A – Minimum and maximum structural width
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  - D – Minimum polysilicon spacing from edge
  - E – Minimum electronics spacing from edge

(c. Carnegie Mellon)
MEMS release step adds new constraints on design rules

CMOS-MEMS Example:

- A – Minimum and maximum structural width
- B – Minimum gap between structures
- C – Minimum structural metal extension
- D – Minimum polysilicon spacing from edge
- E – Minimum electronics spacing from edge
- F – Maximum beam length

Minimum possible gap

- Function of adjacent structural width
- Etch rate depends on local neighborhood

Structural design issues

- Narrow gaps desired for actuation
- Wide structures desired for rigidity and wiring

Desire context-dependent DRC
Process Abstractions: Context Dependent DRC

- Etch rate different for plate and non-plate regions
- MEMS areas recognized by maximum etch criterion
- Released areas found by emulating etch phenomenon

B. Baidya et al., MSM 2001
**Process Abstractions: Layout Parasitic Extraction**

- Circuit Extraction
  - Recognizes layer overlaps and gaps
  - Capacitors, resistors and transistors

- MEMS Extraction
  - Recognizes layer overlaps, gaps and geometrical features
  - Springs, plates, comb drives

**Design Representations**

- 3D Representations
  - Solid Model
  - Mesh
  - Original Design Entry Mode

(c. Carnegie Mellon)
Design Representations

- 3D Representations
  - Solid Model
  - Mesh
  - Original Design Entry Mode
- Layout
  - VLSI fabrication
  - Preferred Design Entry Mode

Design Representations

- 3D Representations
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  - Original Design Entry Mode
- Layout
  - VLSI fabrication
  - Preferred Design Entry Mode
- Behavioral Schematic

Module resonator(vin):

```vhdl
--
parameter real K = 1;
parameter real B = 1e-7;

analog begin
  Pos(Vtop) <+ ddt(Pos(top));
  Pos(Atop) <+ ddt(Pos(Vtop));
  Fe = (V(vin)*V(vin))*area*`eps0/2.0/
      (z0-Pos(top))*(z0-Pos(top));
  F(top) <+ Fe -
         (K*Pos(top) + ms*Pos(Atop) +
          B*ddt(Pos(Vtop)));
end
endmodule
```
Design Representations

- 3D Representations
  - Solid Model
  - Mesh
  - Original Design Entry Mode
- Layout
  - VLSI fabrication
  - Preferred Design Entry Mode
- Behavioral Schematic
- Circuit-level Schematic
- One-on-One Correspondence to Layout

Design Representation Links

Schematic-Driven Layout → Extraction → Circuit-Level Simulation → Schematic-Driven Mesh → Continuum Simulation → Mesh Generation → To Fab

- Continuum Simulation
- Mesh Generation
- Extraction
- Circuit-Level Simulation
- Schematic-Driven Mesh
- Schematic-Driven Layout

- Plate
- Beam
- Comb
MEMS Design Issues

- Will it meet specifications?
  - Dynamic range
  - Sensitivity (parasitics)
  - Sensor resolution (noise)

- Adverse interaction with Interface circuits?
- Electromechanical feedback systems stable?
- Design for manufacturability, testability
  - minimize sensitivity to variations
  - account for device calibration

\[ \sqrt{F_n^2} = \sqrt{4k_BT B \Delta f} \]

Brownian noise

e.g.

Can we answer the design questions?

- Develop a solid model of the geometry
- Mesh it
- Simulate via Finite Element/Boundary Element

Figures courtesy D. Ramaswamy and J. White, MIT (Transducers '99).
3-D Electrostatic and Elastostatic Solvers

- **Electrostatics**
  - Accelerated Boundary-Element Methods (FastCap derivatives)
  - Computes charge distribution given potentials
  - Analyzes whole comb drives in minutes
- **Elastostatics**
  - Nonlinear Finite Element Analysis
  - Computes structure deformation given applied pressure
- **But,**
  - Charge distribution applies pressure on structure
  - Structure deforms, altering the field,
  - Hence charge distribution changes

Coupled Electromechanical Solvers

- Available from: ANSYS, CFDRC, Coventor, Intellisense, ...
  - Relaxation scheme with black-box solvers
  - Or, directly couple the solvers
- Can add more energy domains
  - e.g., thermal, fluidic

![Diagram](carnegie-mellon.png)
Behavioral Modeling ("Macromodeling")

- Low-level physics-based numerical simulation becomes impossible for large problems
  - Simulations are slow and memory intensive
  - Mixed-energy domains ⇒ coupled simulation
- Solution is to partition problem
- Generate analytic equations (explicit equations or ODE’s) for use in higher-level behavioral simulation
- Curve-fit using user-selected basis functions
  - e.g., polynomials, physics-based functions

Bottom Up Design Methodology
MEMS Design Hierarchy

System
- interface circuitry

Device
- transresistance amplifier

Functional element
- op-amp
- plate mass
- spring
- comb sensor

Atomic element
- transistor
- R,C
- plate
- beam
- anchor
- gap

Inertial system

Top Down Design for MEMS

- Methodology for interoperability of models at all levels
- Emphasis on reusable, parametric models
MEMS Model Hierarchy

System models
- Increasing complexity
- Decreasing reusability
- Increasing design cycle time

Device models

Functional element models

Atomic element models

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Circuit-level Modeling

- Models must be
  - Accurate
  - Analytical or ODE representation (lumped)
  - Correct energy conservation and dissipation
  - Models static and dynamic behavior
  - Easy to connect to system-level simulators

- Analog HDLs encodes of models for simulation

- System designer wants design flexibility
  - Identify generally useful components
  - Parameterize components for reuse

Prior/Current Efforts

- NODAS – CMU
  - J. Vandemeer, et al., ASME IMECE’97
  - Licensed to Coventor and MEMSCAP
  - Models in MAST with simulation in Saber
  - Models in VerilogA with simulation in Cadence

- SUGAR – UC Berkeley
  - Models directly in matrices with simulation in Matlab

- ARCHITECT – Coventor
  - G. Lorenz, et al., MSM’98 (originally with R. Bosch)
  - Models in MAST with simulation in Saber
  - Models in VerilogA with simulation in Cadence

- MEMSMASTER – MEMSCAP
  - D. Mouliner, et al., DTIP’01
  - Models in VerilogA with simulation in Cadence
  - Models in Eldo with simulation in Mentor Graphics
Simulation Methodology in NODAS

- Schematically compose structures
- Embedded in commercial EDA tools (Cadence, VerilogA)

![Comb-finger actuator diagram]

\[ \begin{align*}
x_a & \\
y_a & \\
\phi_a & \\
v_a & \\
\end{align*} \]

BEAM
\[ \begin{align*}
L = 10 \mu m \\
w = 2 \mu m \\
\phi = 0 \\
\end{align*} \]

![Comb-finger sensor and shuttle mass]

Output circuit
Resonant direction
Electrostatic comb drive
Input circuit

Behavioral Circuit Modeling

- Models are coupled only through elements’ I/O pins
- e.g., beams and plates are modeled as lumped mass-spring-damper systems

\[
\begin{align*}
dy & = \cos \phi_c \cdot \text{Pos}(y_p, y_m) - \sin \phi_c \cdot \text{Pos}(x_p, x_m); \\
F_{yp} & = m_s/420 * (6*(13*1e6*Aphim-22*1e6*Aphip) \\
& + 54*Aym+156*Ayp)) + dampy*Vyp \\
& + 12*E*Iz/(L*L*L) * (dy - 1e6/2*L*chip_phi); \\
F_{chip_{yp}} & = F_{yp} \cdot \cos \phi_c + F_{xp} \cdot \sin \phi_c; \\
F(y_p) & \leftarrow -F_{chip_{yp}}; \\
\end{align*}
\]
**NODAS**

- **NOdal Design of Actuators & Sensors**
- **Elements (symbols and models) can be reused in new designs**

---

**Simulation**

- **Behavioral simulation in Analog Artist, Spectre**
Simulation

- Behavioral simulation in Analog Artist, Spectre
- All analysis modes available:
  - dc
  - ac
  - parameter sweep
  - Monte-Carlo
  - transient
Mixed-Domain Design Example 1: MEMS Bandpass Filter

**Principle of operation:**

\[ V_{out} = \frac{V_{in}}{Q} \]

\[ \omega = \sqrt{\frac{K}{M}} \]

**NODAS MEMS Circuit**

**Equivalent Linear SPICE Circuit**

Q. Jing et al., MEMS 2000  
K. Wang et al., MEMS 1997  
\[ c. \text{Carnegie Mellon} \]
Mixed-Domain Design Example 1: CMOS-MEMS Bandpass Filter

- NODAS Schematic

- SEM of fabricated device

- NODAS vs. Experiment

Capacitive Accelerometer Basics

- Interface Circuit
- Layout
- Output Waveform
Mixed-Domain Design Example 2: Lateral Accelerometer

- **Layout:**
  - plate mass
  - meander spring
  - capacitive sensor

- NODAS schematic:

![NODAS schematic](image)

Mixed-Domain Design Example 2: Manufacturability Simulation

- **Identical beam widths:**
  - cross-axis sensitivity = 0

- **5% mismatch:**
  - cross-axis sensitivity ~ 10^{-3}

- Transient analysis can be used to predict some failure modes

![Transient analysis graphs](image)
MEMS Circuit Representation: Cantilever Beam Example

**Physics:**

- Anchor:
  - $X = X_1$
  - $Y = 0$
  - $\Theta = 0$

- Beam:
  - $L = 100 \mu m$
  - $w = 2 \mu m$
  - $\Theta = 0$

- Across variables: displacement, angle, voltage
- Through variables: force, moment, current
- Branch relations: $\sum i = 0; \sum F = 0; \sum M = 0$

**Nodal Conventions**

- Across variables ($x, y, \theta_z$ displacement, voltage)
  - Positive valued displacements are in positive axial direction
  - Positive valued angles are counterclockwise around axis

- Through variables ($F_x, F_y$ forces, $M_z$ moment, current)
  - Force flowing into node acts in positive axial direction
  - Moment flowing into node acts counterclockwise around axis

Example: beam in tension

Equivalent schematic:
Behavioral Circuit Modeling

- Primary assumption is that element models are coupled only by nodes
- Beams and plates are modeled as mass-spring-damper systems driven at discrete positions corresponding to the nodes
  \[
  [F] = [m] [\ddot{x}] + [B] [\dot{x}] + [k] [x]
  \]
  \[
  [x] = [x_a \ y_a \ \theta_a \ x_b \ y_b \ \theta_b]^T
  \]
- Electrostatic gaps are modeled as capacitors with moving electrodes
  \[
  C = \frac{\varepsilon_0 A}{g([x])}
  \]
  \[
  [F] = 0.5 V^2 \frac{dC}{d[x]}
  \]
- Implemented in Analogy MAST/Saber and Cadence Verilog-AHDL/Spectre

Sources of Geometric Nonlinearity I: Large Axial Stress Stiffening

- Example: Fixed-fixed beam
- Beam nonlinearity starts at small displacement
- Effective beam length, \( L' \)
- Axial force, \( N \)
Sources of Geometric Nonlinearity II: Large Geometric Deflection

- Example: Cantilever beam
- Beam foreshortening, $x$ and $y$ are coupled
- Force projection into axial stress
- Cubic shape function valid only for small deflection
  - FEA: incremental loading & coordinate update
  - NODAS: coordinate transformation

![Diagram showing effective beam length, $L'$.]

Effective Beam Length, $L'$

**Calculation of $L'$ based on cubic-shape function**

\[ y(x) = f_1(x) y_a + f_2(x) \phi_a + f_3(x) y_b + f_4(x) \phi_b \]

\[ L' = \int ds = \int_{x_a}^{x_b} \sqrt{1 + \left( \frac{dy}{dx} \right)^2} \, dx \]

\[ \delta L = L' - L \]

(f_i(x): cubic shape functions for small displacements)
Axial Force, $N$

- Geometric stiffness matrix, $[K_G]$  
- Calculation of axial force, $N$

$$\begin{bmatrix} F \end{bmatrix} = \begin{bmatrix} K_0 + (K_G(x)) \end{bmatrix} \begin{bmatrix} x \end{bmatrix}$$

$$N(x) \cdot [K_{G0}] = \begin{bmatrix} N \end{bmatrix} = \frac{EA}{L} (x_k - x_b)$$

Geometric stiffness matrix

Modified to:

$$N = \frac{EA}{L} \delta L$$

Ref: Przemieniecki, Theory of Matrix Structural Analysis, 1968

Coordinate Transformations

- Chip frame: specifies layout position
- Local frame: specific to each element
- Displaced frame: shape functions are applied
Dynamic Rotation

- Displacements in local frame are large
- Displacements in displaced frame are small
- Averaging rotations at node $a$ and node $b$

\[
X_{\text{local}} \quad Y_{\text{local}} \quad X_{\text{disp}} \quad Y_{\text{disp}}
\]

Rotation angles in local frame

\[
\phi_x = \frac{(\phi_{ax} + \phi_{bx})}{2} \\
\phi_y = \frac{(\phi_{ay} + \phi_{by})}{2} \\
\phi_z = \frac{(\phi_{az} + \phi_{bz})}{2}
\]

Rotation About an Axis

- General, unique definition

Axis of rotation

\[
\phi = \sqrt{\phi_x^2 + \phi_y^2 + \phi_z^2}
\]

Used to form rotation matrix

\[
\begin{align*}
    p_x &= \frac{\phi_x}{\phi} \\
    p_y &= \frac{\phi_y}{\phi} \\
    p_z &= \frac{\phi_z}{\phi}
\end{align*}
\]

Ref: Glassner, Graphics Gems, 1990
Beam Model Structure

$$\begin{align*}
\begin{bmatrix} x_1 \\ \vdots \\ x_n \end{bmatrix}_{\text{chip}} & \quad \text{KVL: } \sum_{i=1}^{n} x_{i, \text{chip}} = 0 \\
\end{align*}$$

- **In chip frame:**
  - System matrix is built by the simulator (Spectre)
  - Self-consistent solution satisfying KCL and KVL is solved based on network topology

$$\begin{align*}
\begin{bmatrix} x_{\text{local}} \\ \dot{x}_{\text{local}} \end{bmatrix} & \rightarrow \begin{bmatrix} x_{\text{disp}} \\ \dot{x}_{\text{disp}} \end{bmatrix} \rightarrow \begin{bmatrix} F_{\text{disp}} \end{bmatrix}_{\text{disp}} = \left[K \left( x_{\text{disp}} \right) \right]_{\text{disp}} \begin{bmatrix} x_{\text{disp}} \end{bmatrix}_{\text{disp}} \\
\end{align*}$$

$$\begin{align*}
\begin{bmatrix} x_{\text{local}} \\ \dot{x}_{\text{local}} \end{bmatrix} & \rightarrow \begin{bmatrix} F_{\text{local}} \end{bmatrix}_{\text{local}} = \left[B \begin{bmatrix} \dot{x} \end{bmatrix}_{\text{local}} \right]_{\text{local}} \\
\end{align*}$$

$$\begin{align*}
\begin{bmatrix} x_{\text{local}} \\ \dot{x}_{\text{local}} \end{bmatrix} & \rightarrow \begin{bmatrix} F_{\text{local}} \end{bmatrix}_{\text{local}} = \left[m \begin{bmatrix} \dot{x} \end{bmatrix}_{\text{local}} \right]_{\text{local}} \\
\end{align*}$$

$$\begin{align*}
\begin{bmatrix} F_{\text{chip}} \end{bmatrix}_{\text{chip}} & \rightarrow \sum_{i=1}^{m} F_{i, \text{chip}} = 0 \\
\end{align*}$$

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- Process & Design Abstractions
- MEMS Circuit Level Modeling & Simulation
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- Mesh Generation
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Symbol Library

- Low-level elements are:
  - Anchor
  - Beam
  - Plate
  - Gap
  - Comb

Layout Generation

- Automated layout is hierarchically p-cell (parameterized cell) driven directly from elements
Layout Generation Example

- Connectivity derived from schematic

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MEMS Extraction for Layout Verification

- Recognizes layer overlaps and gaps
- Capacitors, resistors and transistors
- Recognizes layer overlaps, gaps and geometrical features
- Springs, plates, comb drives

Previous Work

  - Limited to hierarchical connectivity analysis
  - Verifies pin to pin connectivity of tagged layout
- Does not allow manual layout generation
- Fails to capture parasitics in the integrated layout
Extraction steps

- Input layout geometry
- Canonical representation
- Recognize atomic elements
- Detect functional elements
- Generate schematic

Eg: Folded Flexure Resonator

- Input layout
- Canonical representation
- Atomic elements recognized
- Final extracted netlist
- Simulation using component models
Effect of Mechanical Parasitics

- Layout from layout-generator
- Layout after putting in extra metal in plate

MEMS Parasitics

- Electrical
  - As in VLSI

- Electromechanical
  - Parasitic from released structure to substrate

- Mechanical
  - Metal routes cause additional mass
    - 43% holes, 57% m3, 34.2% m2, 35.91% m1
MEMS Parasitics

- **Mechanical**
  - Joint between beams
    - L: 100μm, w: 2μm
    - L: 100μm, w: 2μm
    - L: 100.6μm, w: 2μm
    - L: 100μm, w: 2μm
    - L: 100μm, w: 20μm
    - L: 2μm, w: 20μm

Extraction Flow

- done using commercial VLSI extractor
- input layout
- separate regions
  - partition MEMS domains
  - extract fluidic MEMS
  - fluidic MEMS schematic
  - extract electrical parasitics in MEMS
  - electrical parasitics in MEMS
- technology library file
- integrated extracted schematic
- stitch schematics
- circuits region
  - extract electrical parasitics in non MEMS areas
  - electrical circuit with parasitics
- extract fluidic MEMS
- extract suspended MEMS
- suspended MEMS schematic
- extract electrical parasitics in MEMS
- electrical parasitics in MEMS
- master extractor
- MAST ER E X T R A C T O R
CMOS-MEMS Extraction

**Problems**
- Multilayer structures
- Etch holes
- O(n^2) algorithms will be too slow

**Solutions**
- Hierarchical bin representation for storage
- Scanline-based algorithms

**More flexibility with electrical connectivity**
- O(n^2) connectivity algorithms will be too slow
- Freedom to design complex types of springs and comb drives

**Mechanical and electrical parasitics**
- Parasitic mass and joints
- Circuit parasitics
- Parasitic capacitances effecting comb drive

**Hierarchical bin representation**

- Layers in canonical form
- Merged layer (MEM layer) + gap layer form bins
- Atomic recognition done on bins
- Merged bins form superbins
- Unrecognized empty bins discarded from superbins
- Functional level recognition done on superbins

B. Baidya et al., MSM 2001
Canonical Representation

- Unique representation for any given layout geometry
- Minimum rectangles covering area between mutually visible parallel edges
  - Non Manhattan geometry will have rectangles and polygons
  - Manhattan geometry will have only rectangles
- Unique neighbor on each edge of resulting polygons and rectangles

![Diagram of canonical representation]

Canonization for Manhattan Geometry

- Simplification possible
  - Only two possible angles
  - Direction of edge can be used to predict its location
  - Final representation has only rectangles
- Only one scan
  - Using only vertical edges
  - Sorted w.r.t x coordinate, y coordinate and direction
  - Scanline drags boxes associated with its edges
  - New edge completes boxes that can be reached on scanline
  - Separate polygonization phase not required
- Simpler and faster than the generalized algorithm
  - Time for creation of boxes = $O(n)$, $n$: final # of boxes
  - Time in operation = $O(\text{elgm})$, $e$: # of edges, $m$: expected # of elements in scanline $\sim O(n^{0.5})$
**Canonization Algorithm (Manhattan) : Example**

- a,b inserted
- c inserted
- box 1 completed
- box 2 dragged
- d inserted
- box 2 completed
- e inserted
- all boxes completed

---

**Canonization (Manhattan): Example**

- folded flexure resonator (using only one structural layer)
- canonized layout (>500 rectangles)
**Canonization (Manhattan): Example**

- CMOS accelerometer (3 metal layers)
- Canonized layout (~50,000 rectangles)

**Z-accelerometer: Parasitic Joints**

- Parasitic joints between short beam
- Width of beam comparable to size of joint
- Extracted schematic of quarter layout
- Layout
Example of Integrated Extraction: Accelerometer

c. Carnegie Mellon

c. Carnegie Mellon
Example of Integrated Extraction: Gyroscope

- Gyroscope
extraction

- Displacement in drive mode
- Displacement in sense mode
- Input rotation

- Output sense voltage of circuit
- Output voltage for common centroid topology (~2μV p-p)
- Output voltage for original topology (~2mV p-p)

- Cross axis coupling at zero external rotation

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Example of Integrated Extraction: Filter

- Extracted schematic matches experimental results more than designed schematic

Context-Dependent Verification

- As in analog VLSI
  - Symmetry is extremely important in MEMS
  - Asymmetry induces mode coupling
    - Noise
    - Common Mode
- Manual interconnections can affect design
- What should be symmetric to what?
  - Easily verified by layout extraction to schematic
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Intelligent Mesh Generation

- Canonical Representation $\Leftrightarrow$ minimal mesh
- Multi-layer CMOS-MEMS mesh generator
  - Recognizes beams, plates, and meshes appropriately

e.g., electrothermal actuator
Curl in CMOS Accelerometer

- anchor
- comb
- rigid frame
- anchor axis
- curl matching

Schematic-Driven Mesh

- Integrates Schematic-To-Layout with Layout-To-Mesh
  - Schematic Source elements become Boundary Conditions

- DC Force
- Anchor
Rigid Elements in MEMS

Proof Mass exhibits rigid behavior

- Treat bulk as a Rigid Body with only 6 degrees of freedom, 3 Euler angles of rotation and 3 displacement variables

Figures courtesy D. Ramaswamy and J. White, MIT (Transducers ‘99).

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Rigid Elastic Formulation

Figures courtesy D. Ramaswamy and J. White, MIT (Transducers ‘99).

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Optimization-based Synthesis

- Design modeling
- Design Optimization
- Design Variable
- Objective
- Device Performance
- Evaluation
- Valid Designs
- No Valid Designs
- Specifications
  - Sensitivity > 20mV/g
  - Noise < 0.1mg/rtHz
- Objective
  - Minimize Area
  - Maximize Range
- Layout Generation
  - Min Area
  - Max Range
- Lumped Parameter Models
- Process
- Manufacturing Variable
- Topology
- Specifications
  - Sensitivity > 20mV/g
  - Noise < 0.1mg/rtHz
Synthesis Approach

Optimization Problem:

\[
\begin{align*}
\text{minimize} & \quad \text{objective}\_\text{function}(X) \\
\text{subject to} & \quad I \leq \begin{bmatrix} X \\ A_{\text{linear}}X \\ c_{\text{non-linear}}(X) \end{bmatrix} \leq u
\end{align*}
\]

Optimization Strategy:
gradient based constrained non-linear optimization

Uses:
» Multiple grid point sampling for initial start-point
» Sequential Quadratic Programming (Lagrange-Newton Method)
» Branch and Bound for integer valued variables
Variables: Plate-mass/Comb-drive

- $W_{\text{stator-finger}}$
- $G$
- $G_1$
- $L_{\text{finger}}$
- $W_{\text{rotor-finger}}$
- $V_{m+}$
- $V_{m-}$
- $W_{\text{pmass}}$
- $L_{\text{pmass}}$
- $L_{\text{beam}}$
- $W_{\text{beam}}$
- $W_{\text{truss}}$
- $L_{\text{truss}}$
- $W_{\text{connect beam}}$
- $L_{\text{connect beam}}$
- $p_{\text{mass}}$

Low Cross-axis Sensitivity $\Rightarrow$ spring symmetry (w.r.t. x axis)

Symmetry $\Rightarrow$ #(truss beams) = ODD

$\Rightarrow$ Use a Thick Connecting Beam

$\Rightarrow$ Constraint: $K_{\text{connect beam}} \geq 10^4 K_{\text{spring}}$
Synthesis: Functional Constraints

- Sensitivity \((slope) > spec\)
- Noise \((resolution) < spec\)
- Offset \(\sim 0\)
- Range \(> spec\)
- Cross-axis sensitivity \(< spec\)
- Bandwidth \(> spec\)

\[\omega_{\text{comb-finger}} < \omega_{\text{modulation voltage}}/1.5\]

\[Sens = \frac{(C_1^0 + C_2^0)}{C_1^0 + C_2^0 + C_{\text{para}}} \frac{m}{k_1} V_g\]

\[Noise = \sqrt{\left(\frac{4k_1 TB}{m}\right)^2 + \left(\frac{\nu_{\text{noise-clk}}}{\text{Sens}}\right)^2}\]

Synthesis: continued

Geometrical Constraints
- Area restrictions
  \((2L_{\text{finger}} + W_{\text{mass}} < X_{\text{size}} < 270 \mu m)\)
- Process design rules
  \((\text{minimum M3 gap} = 0.9 \mu m)\)
- Relative size constraints
  \((\text{e.g., all comb-units must fit on the plate-mass})\)
- Gap constraints for mechanical release
  \((\text{thicker structures need more space around them})\)

Optimization Objectives
- Minimize Noise
- Maximize Sensitivity
- Minimize Area
Synthesis vs. Manual Design

Specifications:
Sensitivity = 0.5 mV/G
Noise ≤ 83 µG/rtHz
Area ≤ 270x500 (µm)²

Optimizes spring design to obtain same sensitivity with less mass & area

<table>
<thead>
<tr>
<th></th>
<th>Manual Design</th>
<th>Minimal Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>Spring Constant</td>
<td>1.56 N/m</td>
<td>0.63 N/m</td>
</tr>
<tr>
<td>Mass</td>
<td>0.56 µg</td>
<td>0.38 µg</td>
</tr>
<tr>
<td>Gap</td>
<td>1.5 µm</td>
<td>1.65 µm</td>
</tr>
<tr>
<td>Area (used)</td>
<td>100%</td>
<td>79%</td>
</tr>
</tbody>
</table>

Synthesis: Maximal Sensitivity

<table>
<thead>
<tr>
<th></th>
<th>Spec</th>
<th>Obtd</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sensitivity(mV/G)</td>
<td>&gt;0.5</td>
<td>1.97</td>
</tr>
<tr>
<td>Range (G)</td>
<td>&gt;50</td>
<td>70</td>
</tr>
<tr>
<td>Noise (µG/rtHz)</td>
<td>&lt;100</td>
<td>100</td>
</tr>
<tr>
<td>Area ((µm)²)</td>
<td>&lt;270x500</td>
<td>100%</td>
</tr>
</tbody>
</table>

Gap = 1.5 µm (= min value)

\[ w_o = 5 \text{ kHz} \]

\[ \text{Limited by area specification} \]
Synthesis: Minimal Noise Objective

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</tr>
</tbody>
</table>

Gap = 2.6 µm (min value is 1.5 µm)
⇒ Squeeze film damping dominant
over other forms of damping

⚠️ Limited by sensitivity specification

Sensitivity vs. Noise Trade-off Analysis

Noise = \sqrt{\frac{4k_BT}{m}} + \left(\frac{V_{meas} - \text{ref}}{\text{Sens}}\right)^2

To right of minimum:
FingerGap ↓ ⇒ Damping ↑ ⇒ Mechanical Noise ↑

To left of minimum:
FingerGap ↑ ⇒ Mechanical Noise ↓, Also Sensitivity ↓ ⇒ Electrical Noise ↑
More MEMS CAD Needs

- Answering additional questions
  - Noise
  - Thermomechanical drift
  - Stress
  - Manufacturing defects

- Design application areas with new physics
  - Optical manipulation
    - Optical
  - Biochemical systems
    - Chemical
    - Fluidic

Conclusions

- Multi-view, multi-level, multi-physics, multi-process design methodology
  - Ability to handle increased complexity
  - Increase in design reuse
  - Decrease in time to working designs
  - Reduction in design errors
  \[\Rightarrow\] Reduce the Design Productivity Gap

- Need
  - Systematic method for process parameter extraction
  - Designer Education
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