Short Course, UIUC, 5/22/2002

Optimizing 10nm-scale Double Gate MOSFET

Sayed Hasan, Jing Wang and Mark Lundstrom
School of Electrical and Computer Engineering
Purdue University, West Lafayette, Indiana 47907-1285

Presented by: Jing Wang *Email:*jingw@purdue.edu

Overview

- Motivation
- Device Structure
- Device Design
- Device Performance
- Discussion
- Summary

1. Motivation

To identify the key challenges in meeting the ITRS targets at the year 2016 and to optimize 10nm-scale Double-gate MOSFET designs using nanoMOS2.0 simulator.

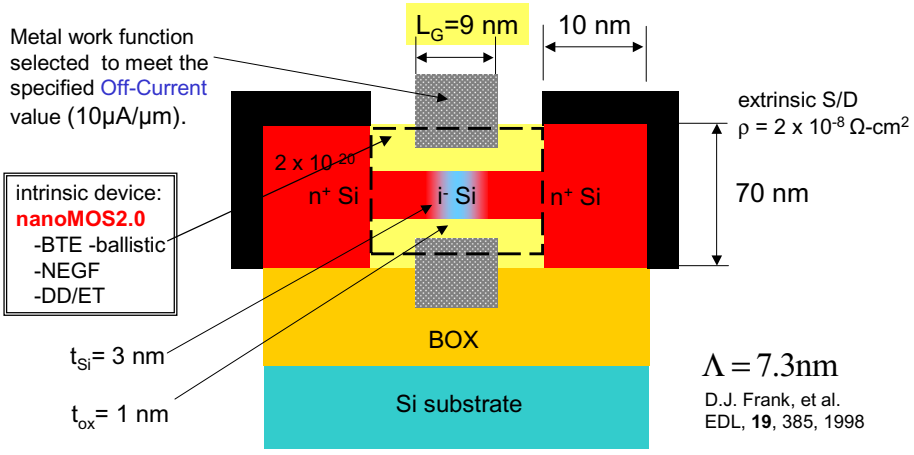
The goals of this project are:

- Exploration of the feasibility of end-of-the-roadmap MOSFETs
- Identification of technology challenges and design approaches

In this talk, we need to focus on the methodology of this study:

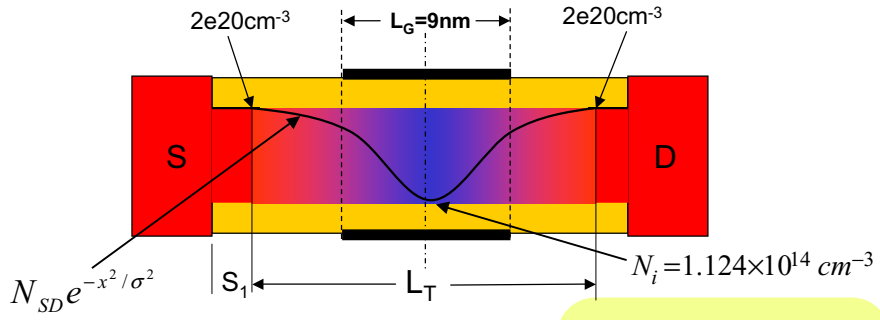
How to use nanoMOS2.0 to design a 10nm Double-Gate MOSFET (High-Performance Device) *?*

2. Device Structure



Taichi Su, J.P.Denton, G.W.Neudeck, *IEEE International SOI Conference, Oct. 2000, pp. 110-111*

2. Structure : Doping



S_1 and L_T are design parameters S_1 set by Miller C

For a specified maximum doping, doping gradient, and I_{off}: examine I_{on}, S, DIBL vs. L_T.

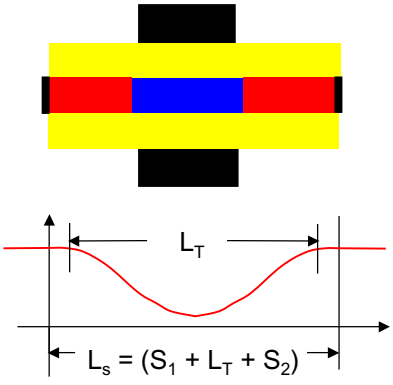
$$g \equiv \left|\frac{dx}{d\log_{10} N}\right|_{\text{At 1 Dec. Point}} = 2\ nm/Dec$$

$$\sigma = 2g\sqrt{\log_{10} e} = 2.636\ nm$$

$$N_i = 1.124\times10^{14}\ cm^{-3}$$

3. Device Design

nanoMOS 2.0



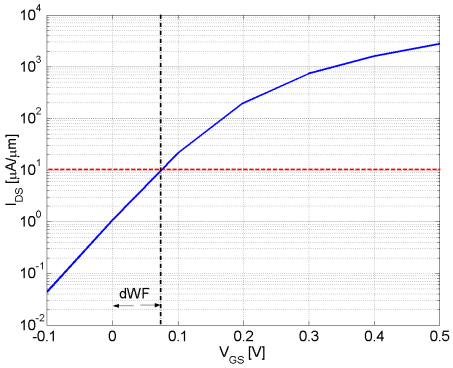
www.nanohub.purdue.edu

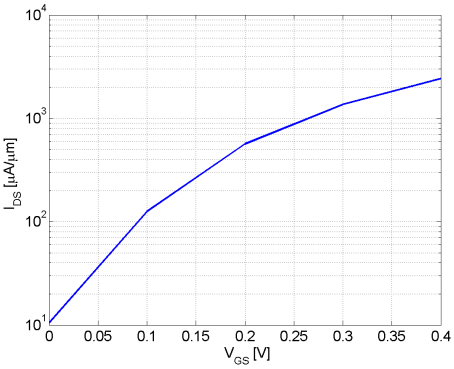
Methodology

1) Select a gate workfunction to give a specified off-current (10μA/μm).
2) Select L_T for maximum I_{on} and DIBL <100 mV/V (BTE - ballistic).
3) Examine sensitivity to L_G and t_{Si}
4) Quantify role of S/D tunneling and gate leakage (quantum-ballistic) *to justify the BTE approach*
5) Explore effects of scattering on channel transport and parasitic S/D resistance. (drift-diffusion)

3. Device Design

How to Select a gate work function to give a specified off-current?



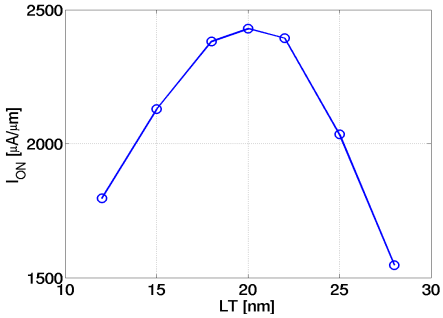


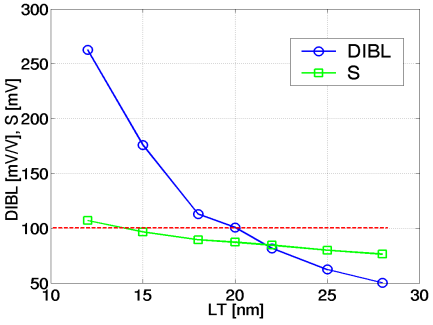
WF_0=4.23eV. I_{off} shound be 10 μA/μm, so dWF=0.07eV. WF_{new}=WF_0-dWF=4.16eV

With WF=4.16eV, I_{off}= 10 μA/μm

3.1 *Design* : Choosing L_T

How to choose an optimized L_T ? – A L_T that can give the highest I_{ON} together with an acceptable S and DIBL





I_{ON} vs. L_T, at I_{off} ~ 10μA/μm

DIBL, S vs. L_T

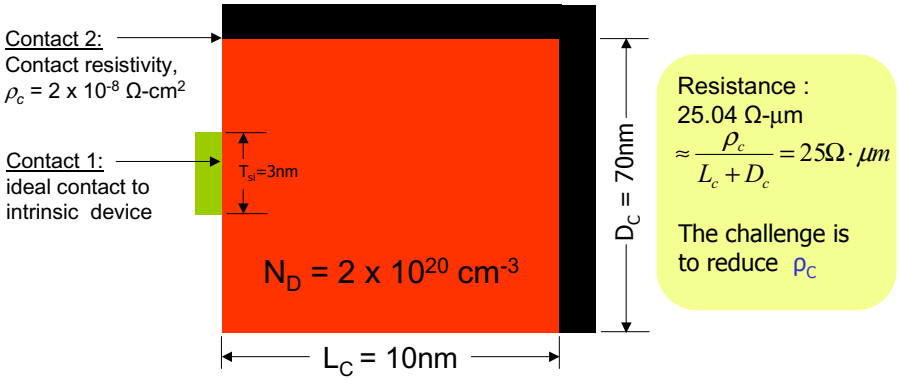
L_T=20nm is the optimized value! (Gate Work Function is 4.16eV.)

3.2 *Design* : input deck

```
$ Example 1$ DEVICE DIRECTIVE
device  nsd=2e20, nbody=0, lgtop=9, lgbot=9, lsd=10,+ overlap_s=-5.5, overlap_d=-5.5,
+ dopslope_s=2.0, dopslope_d=2.0,+ tsi=3.0, tox_top=1.0, tox_bot=1.0, temp=300,

$ GRID DIRECTIVE
grid    dx=0.2 dy=0.2 refine=1

$ TRANSPORT DIRECTIVE
transport model=clbte, mu_low=100, beta=1, vsat=1.8e7, + ELE_TAUW=1e-13, ELE_CQ=1

$ BIAS DIRECTIVE
bias vgtop=0, vgbot=0, vs=0.0, vd=0.4, vgstep=0.1, vdstep=0.1, + ngstep=4, ndstep=0, vd_initial=0.1

$ MATERIAL DIRECTIVE
material wfunc_top=4.16, wfunc_bot=4.16, mlong=0.91, mtran=0.19, kox_top=4.0,
+ kox_bot=4.0, dec_top=3.34, dec_bot=3.34, ksi=11.7

$ SOLUTION DIRECTIVE
solve dvmax=0.001, dvpois=1e-3

$ OPTIONS DIRECTIVE
options valleys=primed, num_subbands=2, dg=true, fermi=true, + ox_penetrate=true

$ PLOTTING CAPABILITES
plots I_V=n, Ec3d=y, Ne3d=y, Ec_sub=n, Ne_sub=n, Te=n, + Ec_IV=y, Ne_IV=y
end
```

3.3 *Design* : S/D Contact Resistance

Design of external S/D using MEDICI

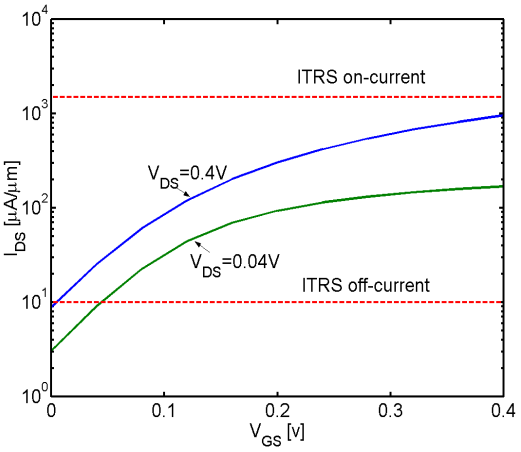


Resistance :
25.04 Ω-μm

$$\approx \frac{\rho_c}{L_c + D_c} = 25\Omega \cdot \mu m$$

The challenge is to reduce ρ_C

4. Device Performance

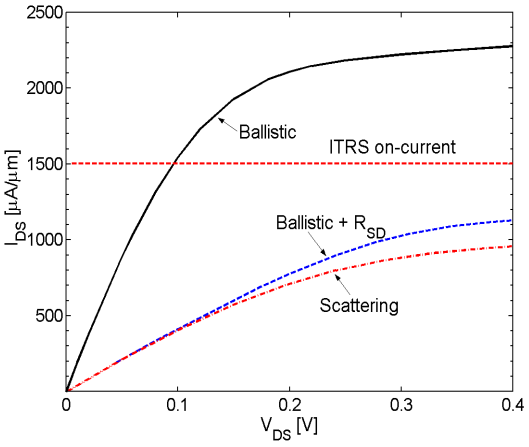


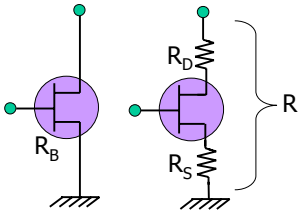
	Value	ITRS
I_{on} (μA/μm)	960	1500
I_{off} (μA/μm)	9	10
DIBL(mV/V)	111	-----
S (mV/dec)	87	75
R_{SD} (Ω-μm)	200	80
V_{DD}/I_{on}	417	267
τ (ps)	0.16	0.15

5. Discussion

1) Parasitic resistance
   --- What is the ultimate limiting factor for the HP MOSFETs?
2) Process variation
   --- Will the current characteristics be sensitive to body thickness and gate length?
3) S/D Tunneling
   --- Is the S/D tunneling effect significant to HP device?

5.1 Parasitic Resistance





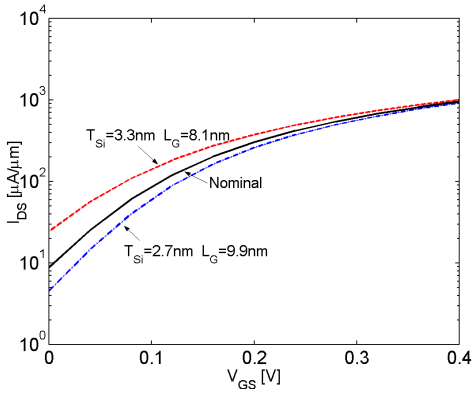
50 0

$R = (R_S + R_D + R_B + R_{CH})$
$= 250\ \Omega\text{-}\mu m$

$R_{SD} \approx (R - R_B) = 200\ \Omega\text{-}\mu m$

$R_{SD} = 2(R_C + R_{tip})$
$= 2(25 + 75)$
$= 200\ \Omega\text{-}\mu m$

5.2 Process Variations



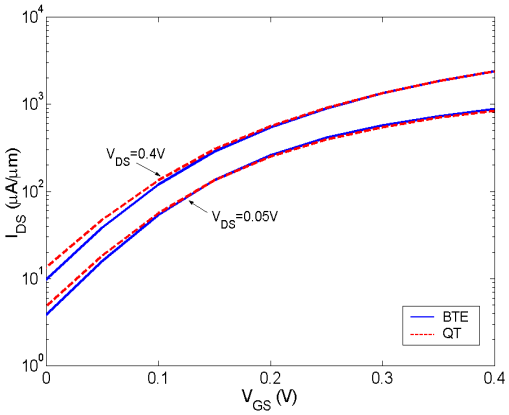
	t_{si} (~10%)	L_G (~10%)
DIBL	26%	24%
S	7%	6%
I_{ON}/I_{OFF}	104%	49%
V_T	42%	10%

For Worst case Design, a little higher gate work function (≈+0.03eV) is needed to make I_{off} equal to 10μA/μm in worst case.

Process Variations due to 10% fluctuation of t_{si} and L_G, *respectively*!

5.3 S/D Tunneling

Nominal Device Structure Simulated by NEGF and BTE



S/D Tunneling Increases I_{OFF} by 30% for High-Performance MOSFET.

Gate Tunneling is negligible for HP Device.

Validity of Classical Ballistic BTE approach is justified.

6. Summary

Procedure of this work:

- *Step 1:* Use BTE model to find the optimized L_T (select different gate work functions to get a specified off-current value of 10μA/μm)
- *Step 2:* Use DD model (NEGF with scattering model for further work) to simulate *intrinsic* device
- *Step 3:* Use MEDICI to calculate S/D contact resistance and then get the current characteristics including parasitic effects
- *Step 4:* Explore S/D tunneling effects (by NEGF model) and other issues that need to be concerned in this study (parasitic resistance, process variation… …).